A prototype for the upgraded read out electronics of TileCal

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This is a collaborative work with the following contributors:

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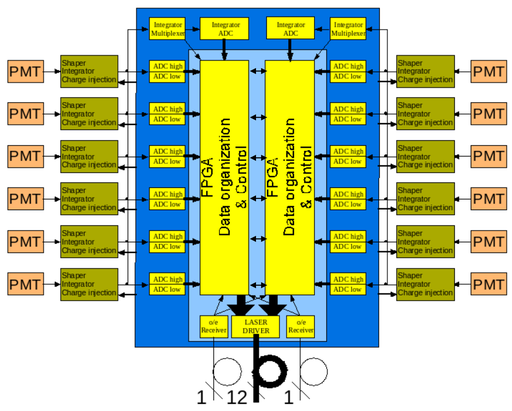
The readout electronics

The future readout electronics will merge the current digitizer, motherboard, mezzanine and interface card, into a two board solution. The first version of the MainBoard will be adapted to the ”3-in-1” front-end alternative. Analog signals from the ”3-in-1” boards are digitized on the MainBoard and transfered to a ”DaughterBoard" with control logic, translation logic and transceivers.



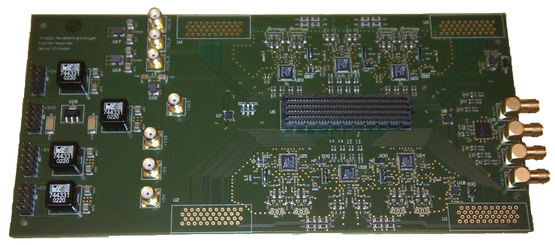
Block diagram of main- and daughterboard layout

The aim is to install one hybrid demonstrator, which is extended to be fully compatible with the present system in ATLAS towards the end of the Phase 0 shut down and potenially three more units during a later yearly shut down. Since the demonstrator have to be compatible with the present system, it must be capable of delivering analog trigger signals and DAQ data in a form acceptable by the present electronics. It must also be able to synchronize and receive commands from the TTC system.

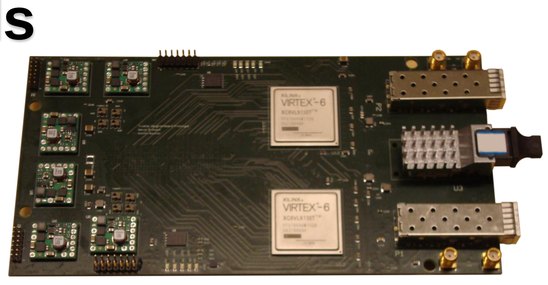
Introduction

Upgrade plans for ATLAS hadronic calorimeter (TileCal) include full readout of all data to the counting room. R&D activities at different laboratories target different parts of the upgraded system. We are developing a possible implementation of the future readout electronics to be included in a full functional demonstrator. This must be capable of adapting to each of three different front-end board alternatives. Prototypes of the two PCBs that will be in charge of digitization, control and communication have been developed. The design is redundant and uses FPGAs with fault tolerant firmware for control and protocol conversion. Communication and clock syncronization between on and off detector electronics is implemented via high speed optical links using the GBT protocol.

The boards



Mainboard



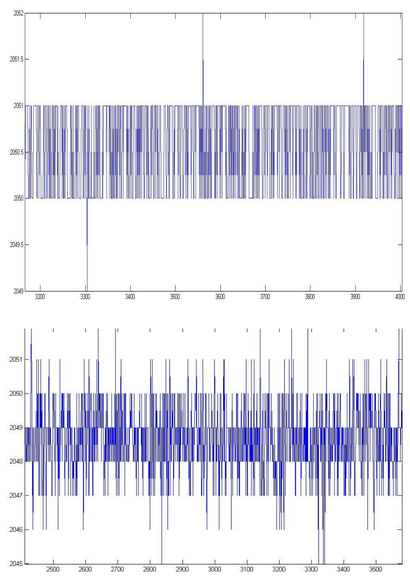
Daughterboard

The purpose of the MainBoard prototype is to provide a reduced size (4 FE channels instead of 12) evaluation platform for the services needed to connect the “3-in-1” front-end boards to the processing and communication facilities on the DaughterBoard. This includes ADCs for digitization, DACs for controlling charge injections and pedestal subtraction.
The board is mirror symmetric around the center line, with two FE board connectors, three ADC's (LTC2264) and one DAC (LTC2634) on each side. A programmable clock distributor with external inputs gives us extended diagnostic possibilities. We are also exploring grounding strategies. The connector to the DaughterBoard is a 400 pin FMC-HPC, giving us the possibility to test this prototype together with off the shelf development boards using the VITA 57 standard.

The DaughterBoard prototype is designed to test the readout system functionality including transmission to the off-detector electronics. It’s also intended to serve future MainBoard prototypes .
We will test the signal integrity of the routing topology and the high speed links. The FPGA will be used to evolve the system firmware. Also, this board is divided into two identical sections for redundancy. The logic is based on Virtex 6 FPGAs (XC6VLX130T), with serial configuration memories. Optical links (2xSFP and one Snap-12) are used to transmit data, commands and signals encoded with the GBT-FPGA protocol[x] at 4.8 Gb/s/link. Synchronous operation is achieved by extracting a global clock from the received GBT signal.
MainBoard data is duplicated on the DaughterBoard for the two FPGAs using a multipoint topology to reduce connections between the boards.

x) Optimizing latency in Xilinx FPGA implementations of the GBT

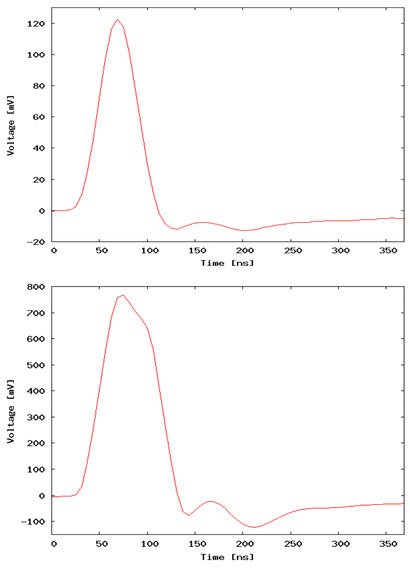
Early test results



Offset readout of 16000 samples from the Mainboard ADC, showing noise levels:

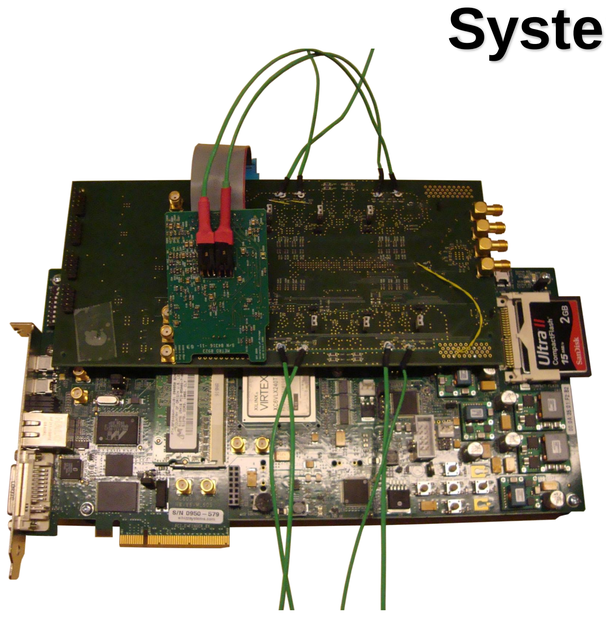
Low gain channel

High gain channel

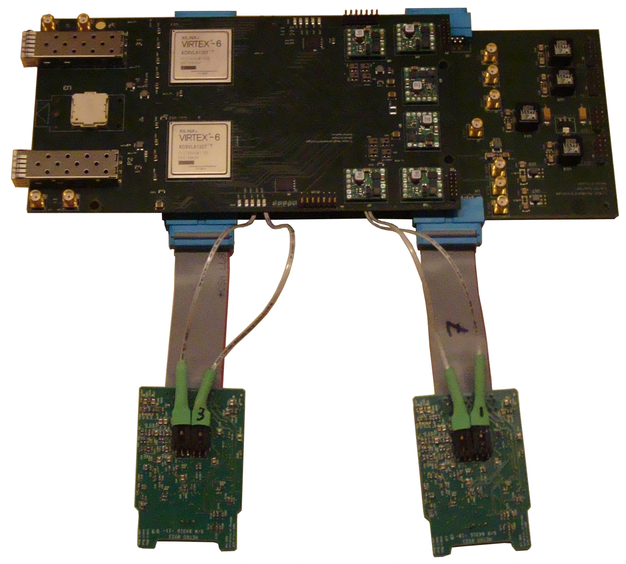


Composite of four pulses, 90° phase shifted, successfully sampled from the 3-in-1 boards and read out with Chipscope. Low gain and high gain.

System assembly



MainBoard with ML605



MainBoard with DaughterBoard

Comments

The early results shown have been obtained before tweaking parameter choices that have been left open to allow design optimization (some termination values, filters etc). So there is surely room for reducing noise and further improve wave forms.

The processing have been done with the set-up based on the Xilinx ML605 board shown above on the left. Tests of the MainBoard/DaughterBoard combination on the right has been initiated.