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A prototype for the upgraded read out electronics of TileCal

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Upgrade plans for ATLAS hadronic calorimeter (TileCal) include full readout of all data to the counting room. We are developing a possible implementation of the future readout and trigger electronics aiming at a full functional demonstrator during Phase 0, starting from an existing functional test slice assembled using a combination of prototypes and emulators. Presently the first version of two PCBs in charge of digitization, control and communication are being developed. The design is highly redundant, using FPGAs with fault tolerant firmware for control and protocol conversion. Communication between on and off detector electronics is implemented via high speed optical links.

Summary 500 words

To upgrade the current TileCal front end electronics and implement new functionality, the plan is to merge the current digitizer, motherboard, mezzanine and interface card, into a two board solution. Based on a possible analog front-end readout electronics board (3-in-1 board) solution [1], a “mainboard” including analog parts, and a “daughterboard” with control logic, translation logic and transceivers is under development. The long term aim is to build one fully functional demonstrator with the required functionality to be verified in test benches and later installed in ATLAS towards the end of the Phase 0 shut down. If the first unit operates as expected three more units may be installed during a later yearly shut down. To achieve this, the demonstrator must be compatible with the present system. Apart from its new functionality it must be capable of delivering analog trigger signals and DAQ data in a form that can be accepted by the present electronics. It must also be able to synchronize and take commands from the TTC system.

The daughterboard logic is based on Virtex 6 FPGAs, which have already been used in an early emulation of a readout slice [2] aimed at studying system and firmware issues. Here off the shelf development boards have been used to study the functionality of the demonstrator. High speed optical links are used to transmit data, commands and signals encoded with the GBT-FPGA protocol at 4.8 Gb/s. The synchronous operation of this readout slice was, as required, achieved by using one global clock signal distributed over the entire design.

To ensure radiation tolerance, eventually the entire on detector part must be exposed to relevant radiations to verify that it can survive in its intended environment and recover from single event upsets. Several components have already been tested. E.g. testing the FPGAs and making sure that the firmware can handle single event upsets remains to be done. Radiation tolerance on the logical level will be ensured by using techniques like for example triple mode redundancy, which has been preliminary implemented and tested.

A crucial feature of the demonstrator is the in system programmability (ISP). This will give us the possibility to test and upgrade designs as well as a way to recover from errors in the configuration memories due to radiation. The final demonstrator will probably use one GBTX for this purpose.

Although most of the hardware components are still under development, large parts of the firmware for the demonstrator as well as the test bench are already implemented and tested, providing a platform that allows the fast and uncomplicated verification of the functionality of new hardware.

Experiences and early performance results will be reported.

References:
[1] F. Tang, Design of the Front-end Readout Electronics for ATLAS Tile Calorimeter at the sLHC, accepted for publishing at IEEE Transaction on Nuclear Science

[2] S. Muschter, A Full Slice Test Version of a Tentative Upgraded Readout System for TileCal, Common ATLAS CMS Electronics Workshop for LHC upgrades, February 2011, Cern

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