Contribution ID: **135** Type: **Poster**

# Architectural modeling of pixel readout chips Velopix and Timepix3

*Thursday 29 September 2011 16:00 (2h 30m)*

We examine two digital architectures for front end pixel readout chips, Velopix and Timepix3. These readout chips are developed for tracking detectors in future high energy physics experiments. They must incorporate local intelligence in pixels for time-over-threshold measurement and sparse readout. In addition, Velopix must be immune to single-event upsets in its digital logic. The most important requirements for both of the chips are pixel size, timing resolution, low power and high-speed sparse readout. We describe the transaction level architectural models of the chips using SystemVerilog after which we refine these models to register-transfer level. The correctness of the models is ensured using Open Verification Methodology. We will also discuss the advantages gained from transaction level modelling.

## Summary 500 words

The performance requirements of tracking in high-energy physics (HEP) require more efficient tracking detectors. To answer the challenge posed by the tracking applications, the number of digital circuits in the pixel readout system-on-chips (SoCs) is increasing. The increased number of digital functions complicates tracking detectors requiring more advanced design and verification methodologies. Therefore, the architectural exploration of the digital circuits is performed at the transaction level. The transaction level architectural exploration is one of the most important parts of the design process because a significant fraction of the performance, area and power consumption of SoCs are defined at this level. Power is especially important as heat extraction in these applications is extremely difficult.

We examine two tracking detector SoCs, namely Velopix for the LHCb upgrade and Timepix3 which is a general purpose particle detection chip. Both of the chips require data-driven architectures without any external trigger. Data sparsification is also necessary to maximise the use of existing on-chip bandwidth. Velopix detects and tags hits in time with 25ns resolution. Pulse height information is required to improve the tracking resolution and this is achieved using time-over-threshold (ToT) technique with a range of 4 bits. To minimize digital logic, the concept of a super pixel has been introduced where an array of 4x4 pixels will share resources such as control logic. To reduce the overall data rate, zero suppression and clustering are done within the super pixel, which then transmits a data packet of varying length depending on the hit occupancy of the 4x4 pixels. More resources are shared within a group of 4 super pixels, and there is one readout unit per group connected to an 8-bit column bus clocked at 40 MHz. The full chip consists of 64 super columns, each of 16 groups of 4 super pixels. Correspondingly, the periphery of the chip has 64 End-of-Column (EoC) blocks connected to a hierarchy of buses and intermediate FIFOs driving the outputs of the chip.

Timepix3 detects and tags hits in time with coarse (25ns) and fine (1.67ns) resolutions, and a ToT range of 10 bits on a pixel level. Each pixel individually detects the hit but the readout functionality is shared between an area of 2x4 pixels. A data packet consists of data from one pixel only. The readout block is connected to a column bus of 160 Mbps. The full chip consists of 128 super columns of 64 super pixels, each containing 8 pixels. The digital periphery of the chip has 128 EoC FIFOs each connected to a token arbitrated bus of 2.56 Gbps.

In designing the new pixel readout chips, we apply object-oriented design and verification methods at the transaction level to quickly verify different architectural models against the specifications of Velopix and Timepix3. An architectural model of Velopix was developed first at the transaction level using SystemVerilog (SV). SV enables a high level description of a configurable super pixel, column bus architecture, arbitration and EoC blocks connected to a periphery bus as well as output serializer blocks. By re-using this model, a full architecture for Timepix3 was quickly established. In re-use, most of the blocks from Velopix were used in Timepix3 with little or no modifications at all, although the chips are different in granularity of the functionality of hit detection (super pixel level versus pixel level). This was possible by using highly abstract transaction level description of arbiters and buses and by encapsulating a chip specific data into packets. Owing to similarities in the architectural structures of pixel readout chips, it is advantageous to develop a standard transaction level model for these chips. The transaction level architectural models can then be used as functional reference models in the verification of register-transfer level (RTL) models using Open Verification Methodology. The used methods have been presented and used in industry for a number of years, but are only now being adopted for SoC design in HEP applications.

The pixel readout SoCs are being designed in 130nm CMOS process using a combination of a standard cell library, a custom cell library and full custom analog design. The development of these architectures has benefitted from TLM in terms of the design space exploration and debugging can be carried out much faster than with RTL modelling.

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**Session Classification:** Posters

**Track Classification:** ASICs