Power network impedance effects on noise emissions of DC-DC converters

M. C. Esteban, F. Arteche, M. Iglesias, I. Vila, F. J. Arcega

a Technological Institute of Aragon, María de Luna 8, E-50018 Zaragoza, Spain
b IFCA, Instituto de Física de Cantabria, Santander, Spain
c Universidad de Zaragoza, Zaragoza, Spain
cesteban@ita.es

Abstract
The characterization of electromagnetic noise of DC-DC converters is a critical issue that has been analyzed during the design phase of CMS tracker upgrade. Previous simulation studies showed important variations of conducted emission of DC-DC converters among impedances and power network topologies. Several tests have been performed in real DC-DC converters to validate the Pspice model and simulation results. This poster presents these test results. Conducted noise emissions at the input and at the output form DC-DC converters have been measured for different types of power network and FEE impedances. Special attention has been paid in the influence of carbon fiber in the CM noise emissions. The results of these studies show important recommendations and criteria to be applied to integrate the DC-DC converters to decrease the system noise level.

Motivation
New FEE requirements forces to install DC-DC converters close to FEE:
- DC-DC converters are a noise source: it is necessary to minimize the total noise inside sub-detector volume.

Network noise variations on noise emissions of DC-DC converters is important to estimate the electromagnetic environment of CMS tracker upgrade system.

CMS Tracker upgrade power network impedences

Input
Low impedance in DM
- Large amount of capacitors connected in the Power Network
Possible grounding will be define:
- Detector or negative line has to be grounded due to safety reasons & performance.
- At high frequency "stray capacitance" starts to play an important role

Output
- Decoupling capacitors: Each DC-DC supplies to several chips
- Stray capacitances define the CM impedance
- Cooling blocks close to the DC-DC
- Frame support is made of Carbon Fiber
- Similar to copper above 500 kHz.

Impedance effects on noise emissions of DC-DC converter: Differential mode noise

Noise emissions system test set-up

A test board has been designed to represent the power network impedances

Real test set-up: Double stack configuration

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