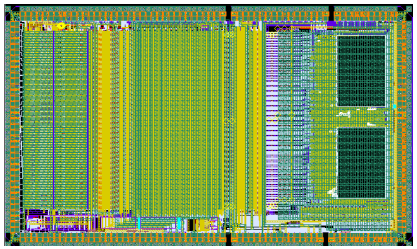
SKIROC2

Silicon Kalorimeter Integrated Read-Out Chip

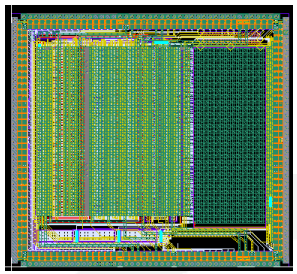
Stéphane CALLIER, Christophe DE LA TAILLE, Frédéric DULUCQ,
Gisèle MARTIN-CHASSARD, Nathalie SEGUIN-MOREAU

Orsay MicroElectronics Group Associated

ROC chips for ILC prototypes

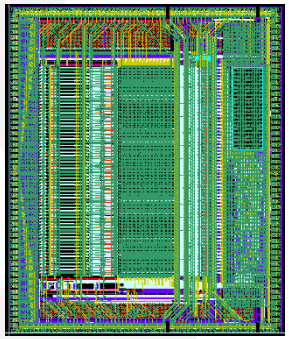


SPIROC2
Analog HCAL (AHCAL)
(SiPM)
36 ch. 32mm²
June 07, June 08, March 10

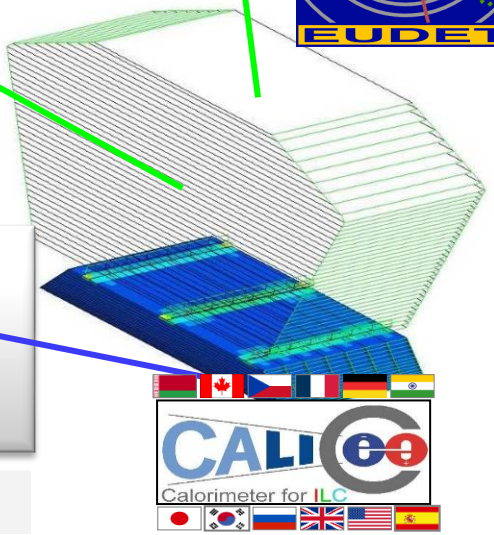


HARDROC2 and MICROROC
Digital HCAL (DHCAL)
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06, June 08, March 10

Microroc: Poster ID-44



SKIROC2
ECAL
(Si PIN diode)
64 ch. 70mm²
March 10



- ROC chips for **technological prototypes**: to study the feasibility of large scale, industrializable modules (Eudet/Aida funded)
- Requirements for electronics
  - Large dynamic range (15 bits)
  - Auto-trigger on ½ MIP
  - On chip zero suppress
  - **10^8 channels**
  - Front-end embedded in detector
  - **Ultra-low power : 25µW/ch**

EUDET/AIDA ECAL technological prototype

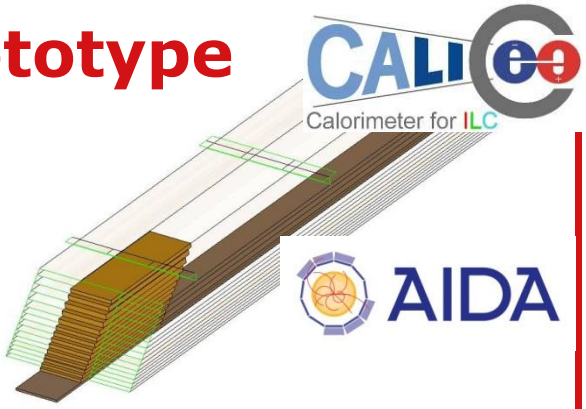
- « Imaging » calorimetry for « particle flow algorithm » => 30%/√E jet resolution
  - **High granularity and segmentation of the calorimeters**

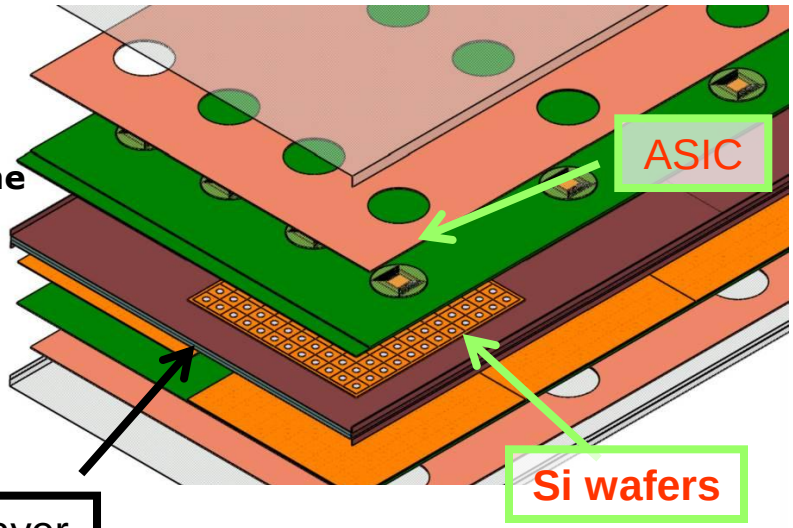
- ECAL: **Si W Calorimeter**
  - **Active medium: SILICON SENSORS (WAFERS)**
  - 325µm thick Silicon Wafers => 26000e⁻/MIP ie 1MIP=4.2 fC
  - High granularity : **5.5x5.5 mm²**
  - High segmentation =>
    - **45 000 cells with embedded electronics for the technological prototype**

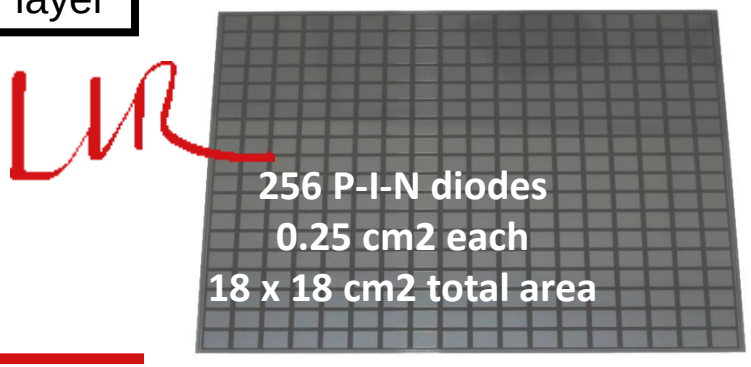
- Final ECAL: 30 layers, **100 M channels**
  - **SKIROC2 embedded** inside the detector
  - **No (few) external components**

- "stitchable" motherboards (Active Sensor Units)
  - Minimize connections between boards

- Low cost and industrialization are the major goal





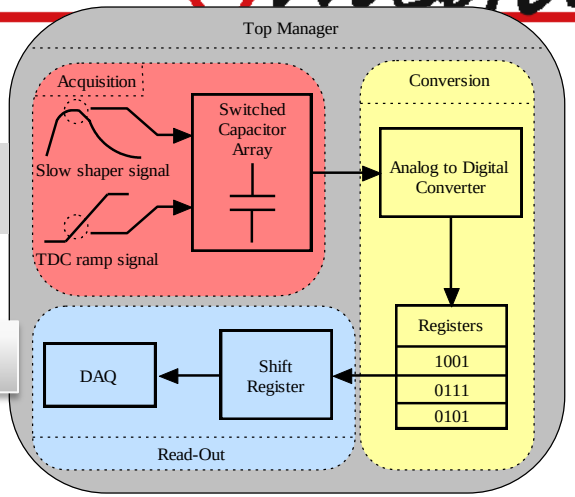


COMMON READOUT: TOKEN RING Mode

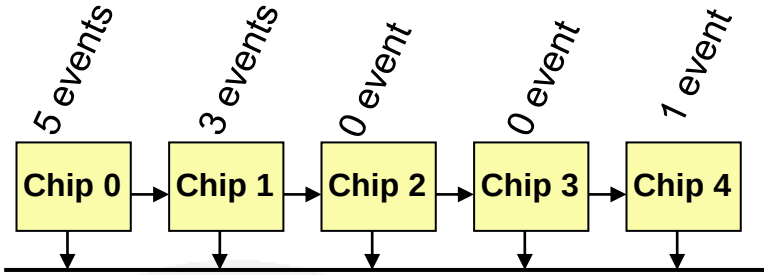
Readout architecture **common to all calorimeters** and **minimization of data lines & power**

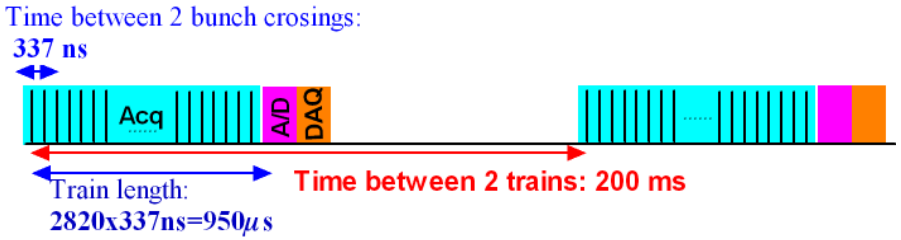
- **Daisy chain** using token ring mode
- Open collector, low voltage signals
- Low capacitance lines

SCA in SK2 and Spiroc

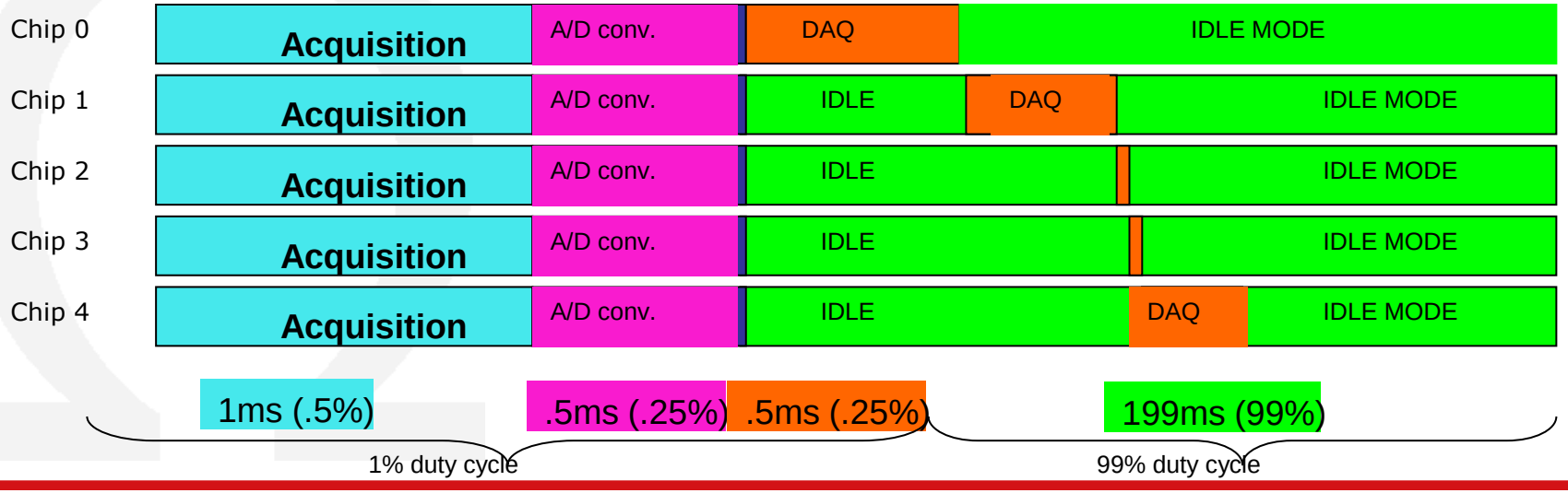


DAQ: Poster ID-109



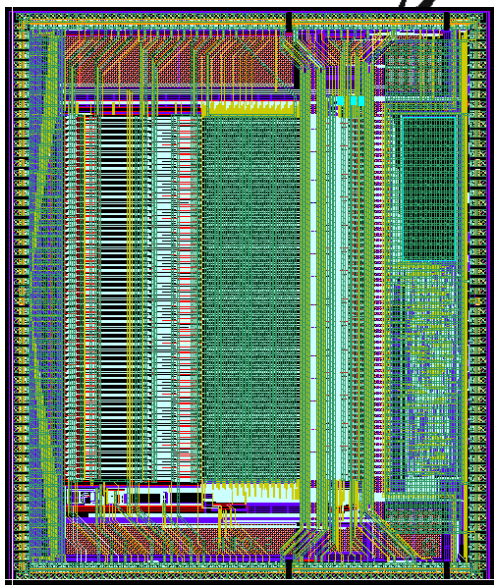


Data bus



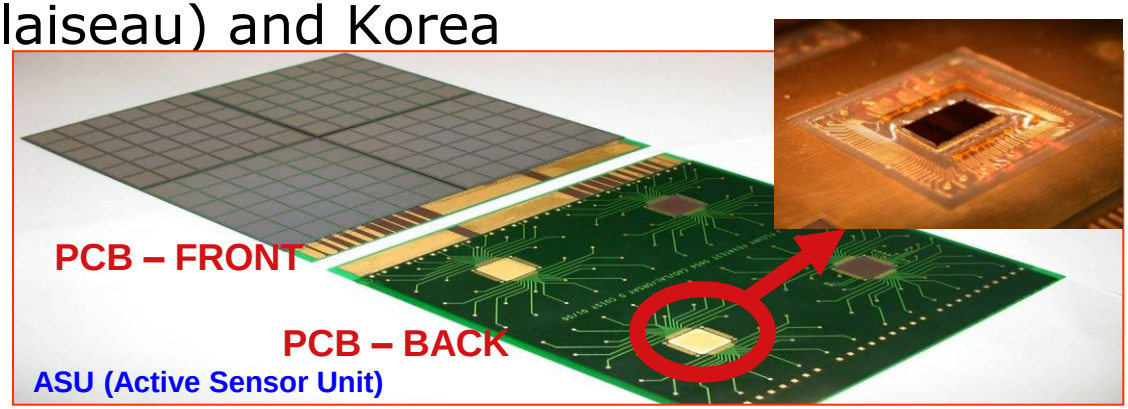
SKIROC : ECAL readout

- SKIROC2 : Silicon Kalorimeter Integrated Read-Out Chip
  - 64 channels, AMS SiGe 0.35 µm, 70 mm^2
  - **Very large dynamic range**:
    - HG for 0.5-150 MIP, LG for 150-2500 MIP
  - Auto-trigger, Analog storage, Digitization & Token-ring ReadOut
  - Testability at wafer level



- Front End boards crucial element
  - Collab with LLR (Palaiseau) and Korea

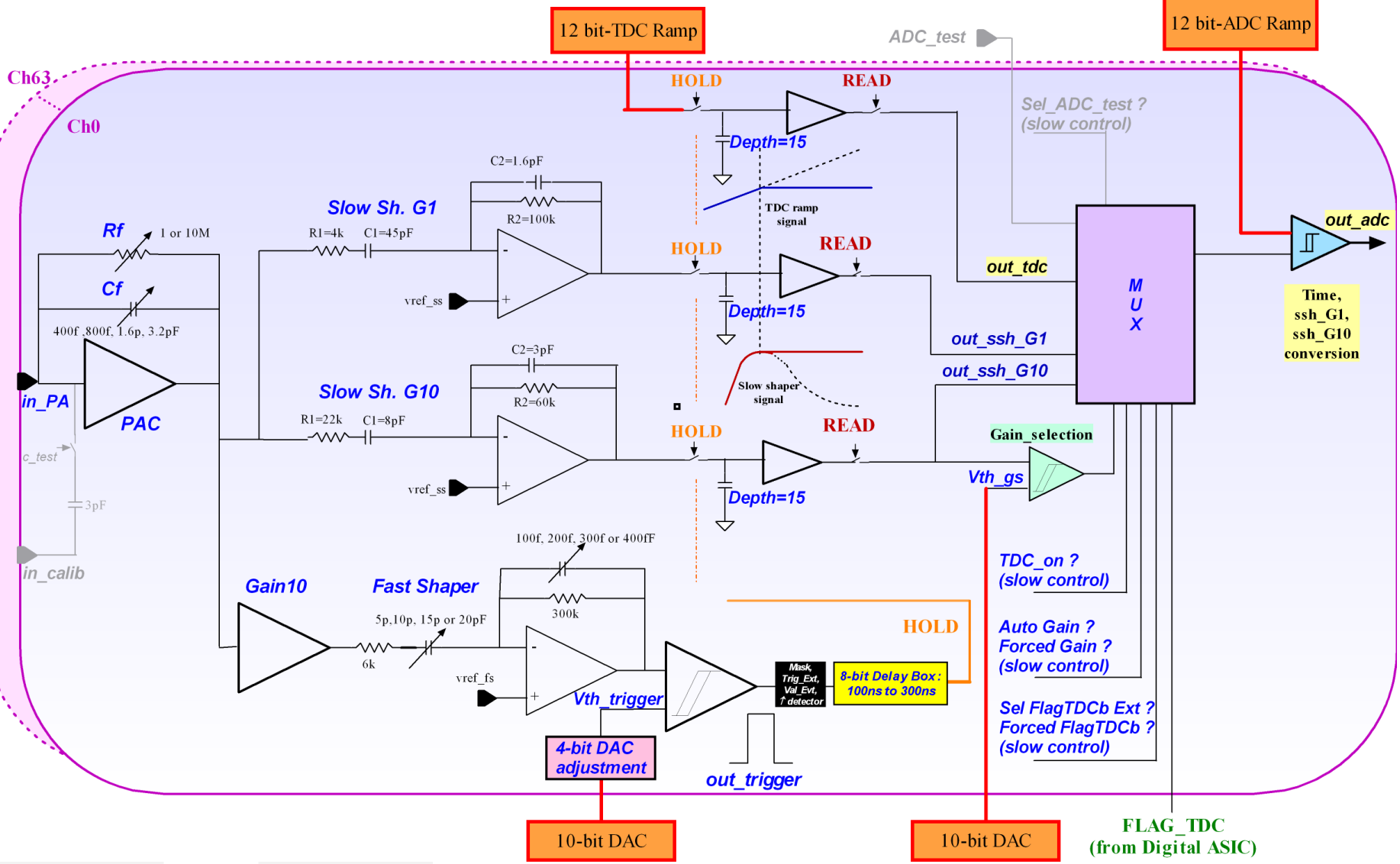
C detector with PCB ≈ 20 pF



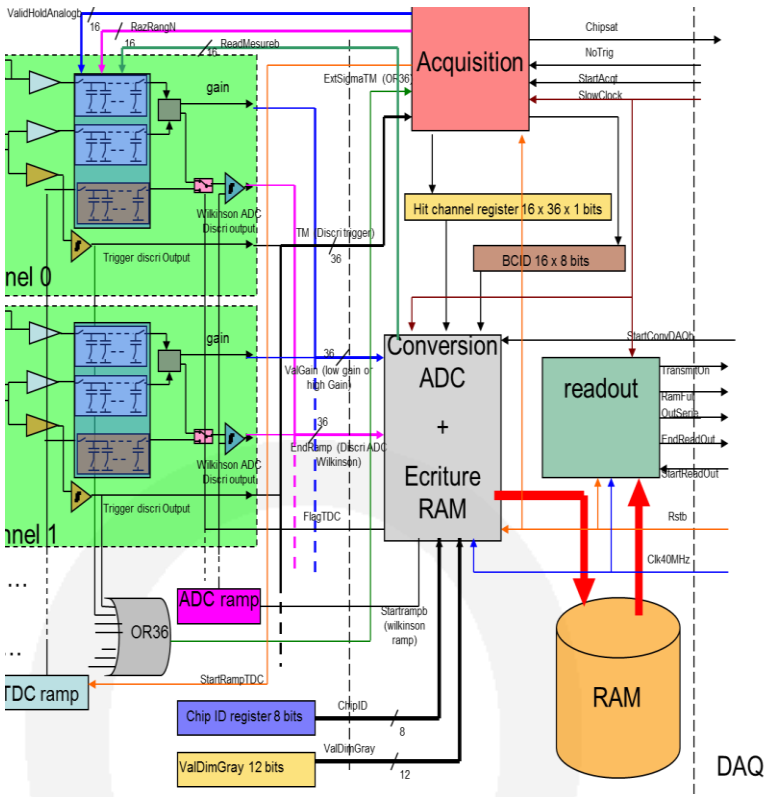
SKIROC2 features

- Very low noise (0.4 fC = 2 500 e-) and very large dynamic range (2fC up to 10 pC) charge preamplifier
- 180ns shaping time Slow Shapers for charge measurement
- 2-bit shaping time adjustable Fast Shaper (50 to 100ns)
- 10-bit DAC for discriminator threshold , With 4-bit adjustment on each channel
- Analogue Memory depth : up to 15 events can be stored
- Trigger Discriminator for autotrigger on ½ MIP
- 8-bit adjustable delay to position the Hold signal
- Digitization of either time and charge or of both charges

SKIROC2 Analogue core



SKIROC2 digital features

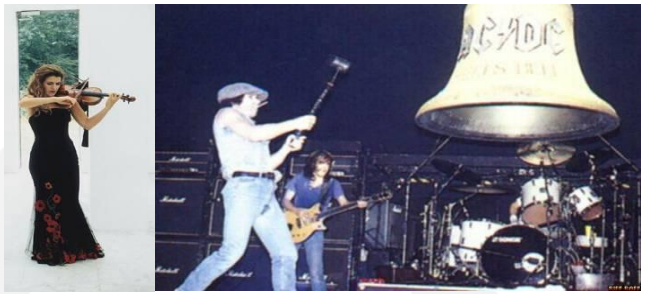


- Common features with Hardroc & Spiroc (compatibility with any CALICE DAQ system)
  - Open Collector token-ring ReadOut
  - Multiplexed Slow Control & Probe
  - Redundancy on Data Out & Transmit On signal lines
  - 2 switchable StartReadOut Inputs & EndReadOut Outputs :
    - to prevent chip failure
- Very Complex Digital Part (~10% of the Die)
  - Manage Acquisition, Conversion, 15 SCA control, RAM, I/Os…

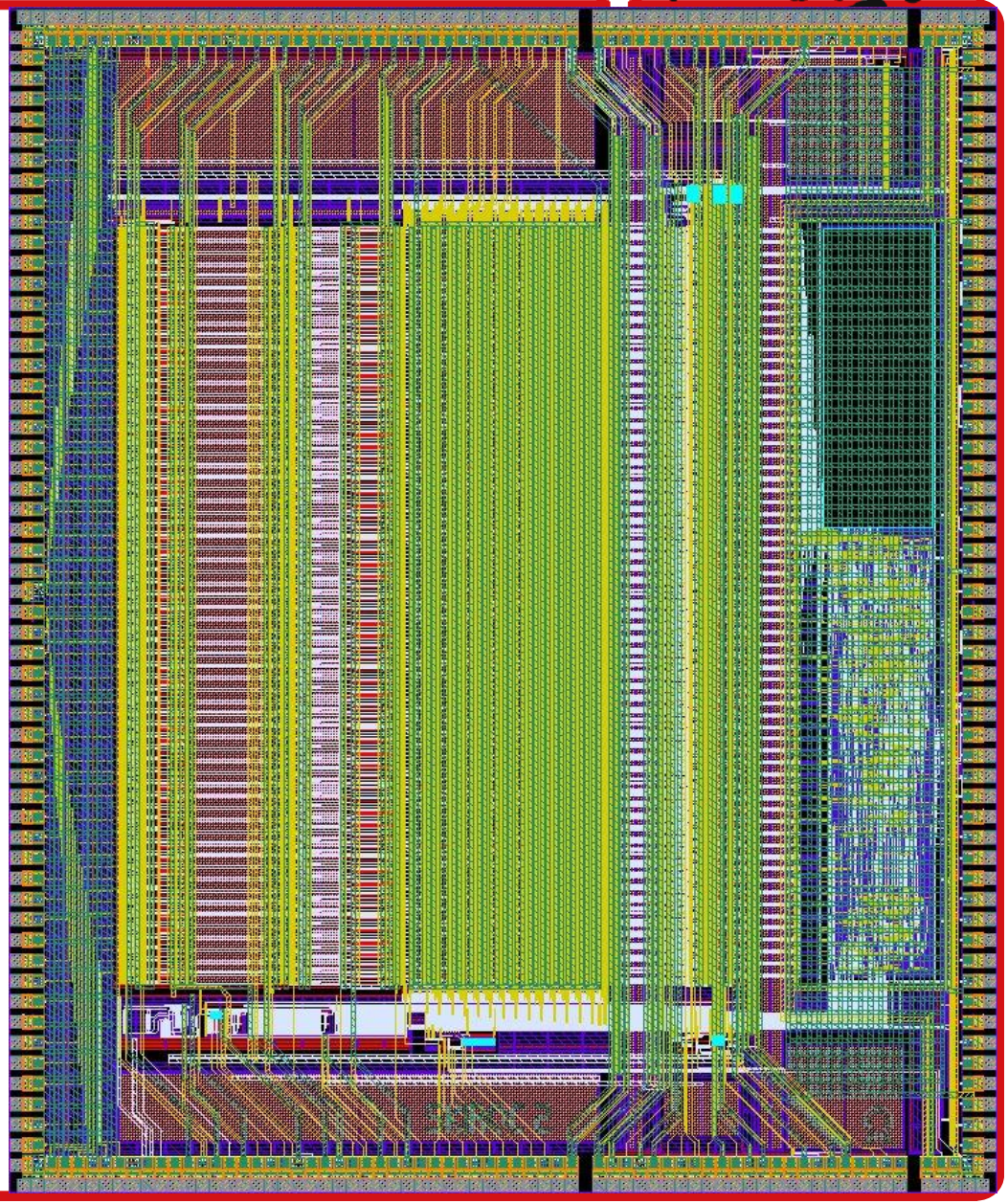
SKIROC2 overview

S*ilikon*
K*alorimeter*
I*ntegrated*
R*ead*
O*ut*
C*hip*

- 64 Channels
  - Difficult layout: 1Mip=4fC, digital activity

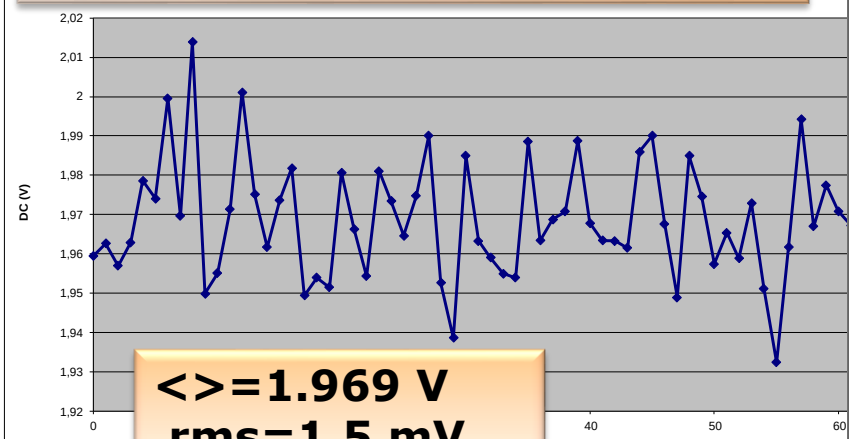


- 250 pads
  - **17 for test purpose only**
- AMS 0.35 µm SiGe
- Die size = 65 mm²
  - 7.5 mm x 8.7 mm



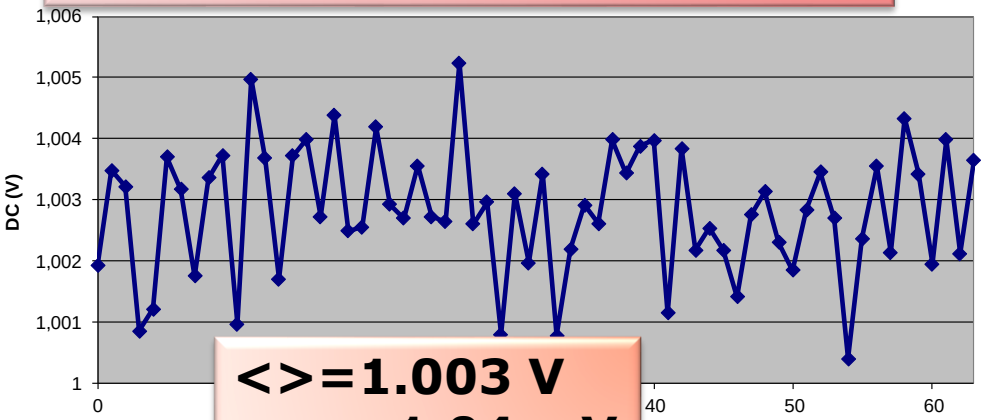
SKIROC2:DC PreAmp, Fast and Slow Shapers

Out_PA: uniformity of the DC level



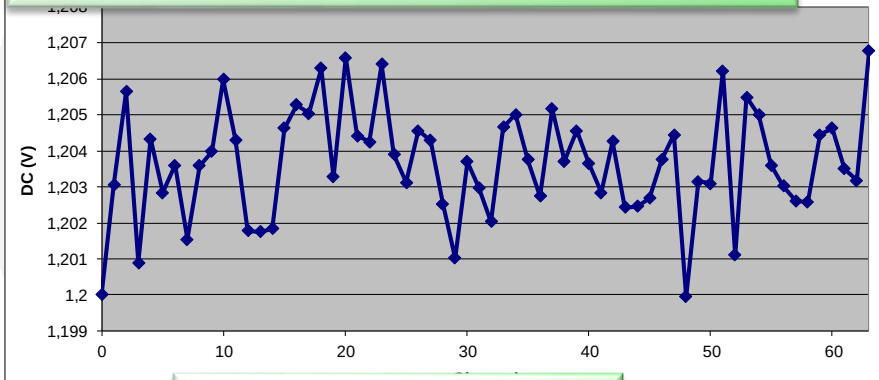
<>=1.969 V
rms=1.5 mV

Out_SS10: uniformity of the DC level



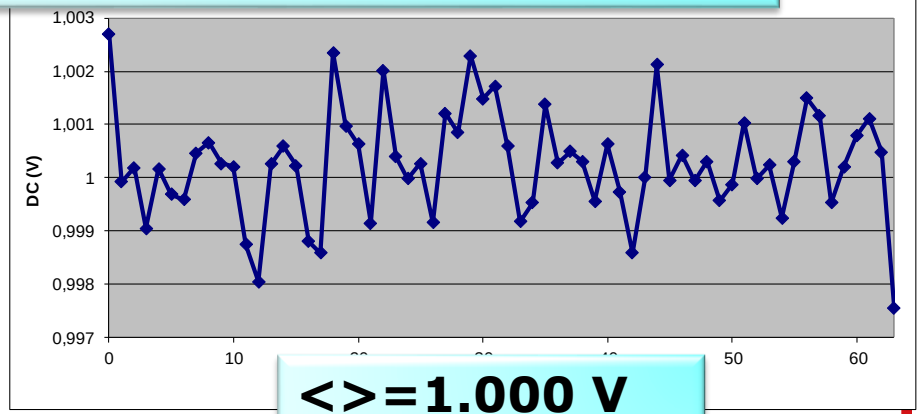
<>=1.003 V
rms=1.04 mV

Out_FS: uniformity of the DC level



<>=1.204 V
rms=1.5 mV

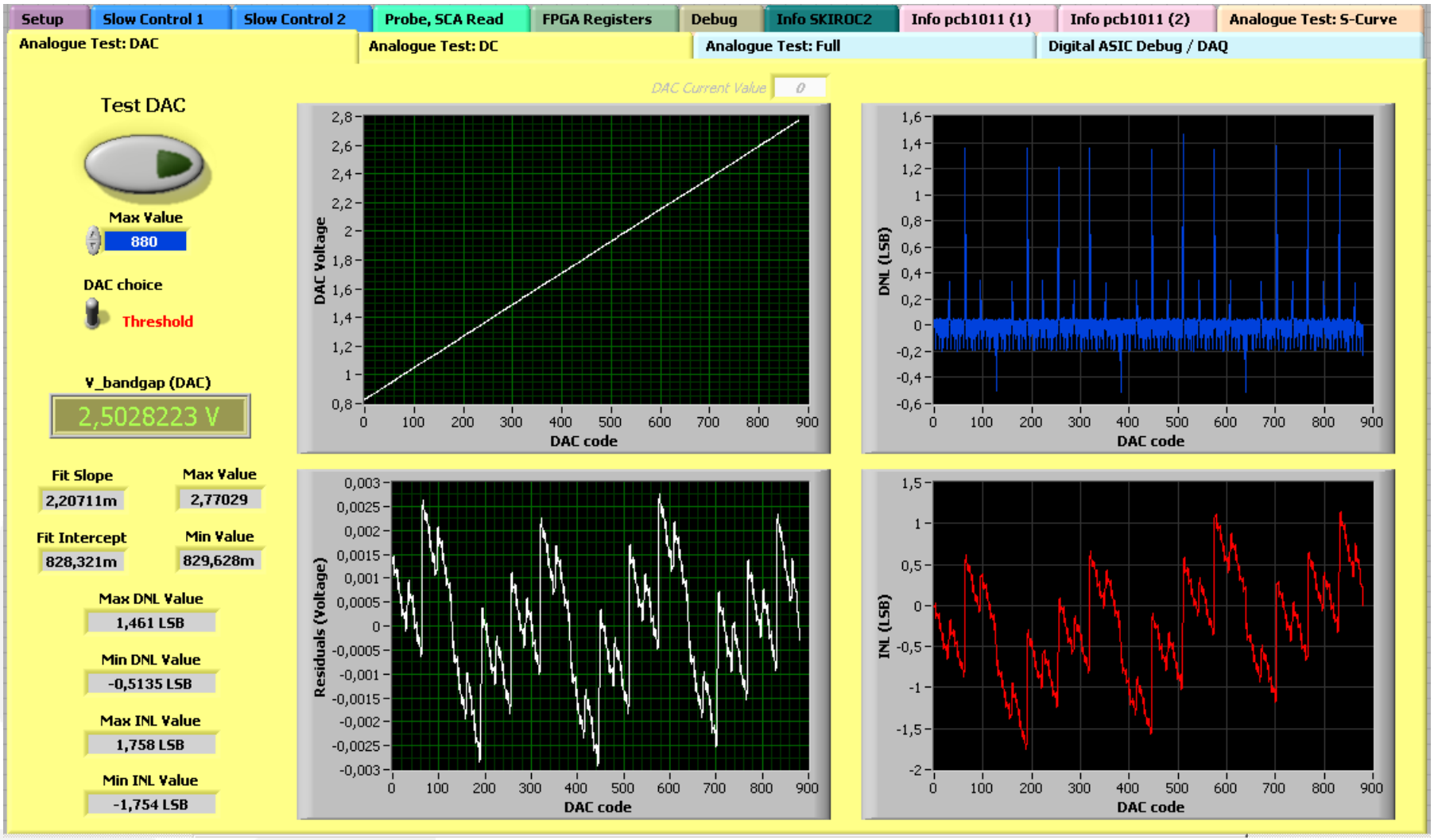
Out_SS1: uniformity of the DC level



<>=1.000 V
rms=1.00 mV

DAC Threshold Linearity

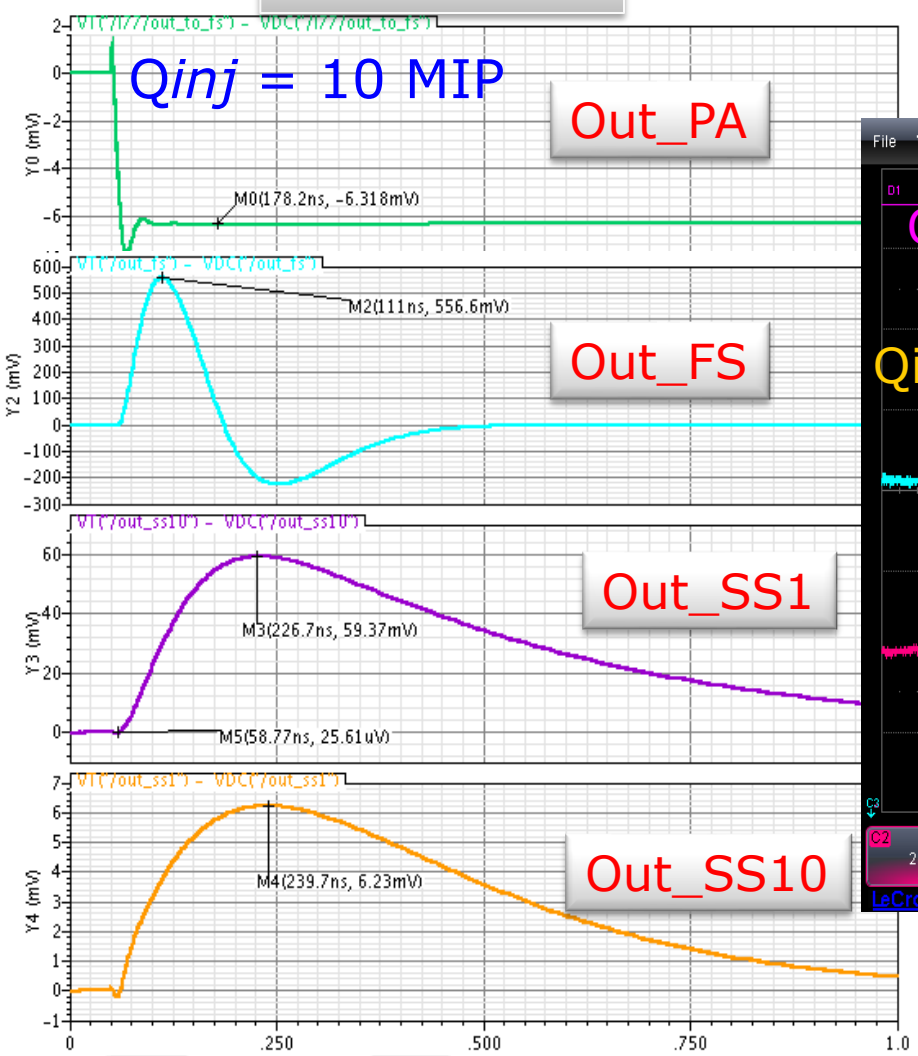
Slope 2.2 mV/DAC Unit, DNL ±1LSB INL= ±1.7LSB

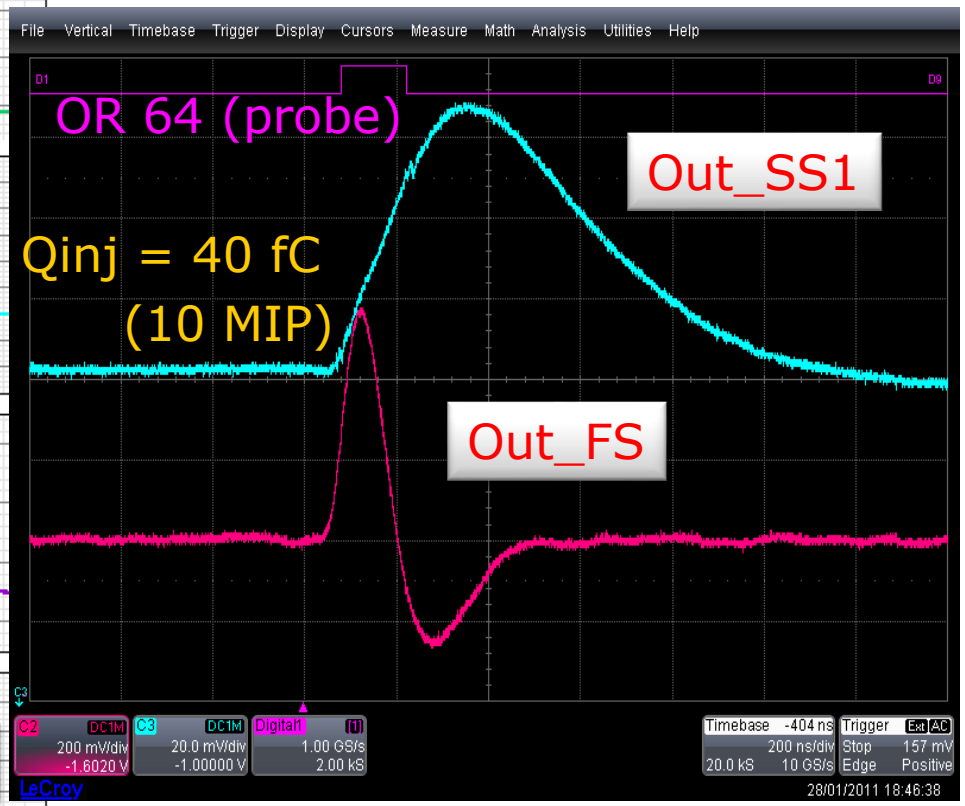


SKIROC2 Analogue Simulations/Measurements

SIMULATIONS

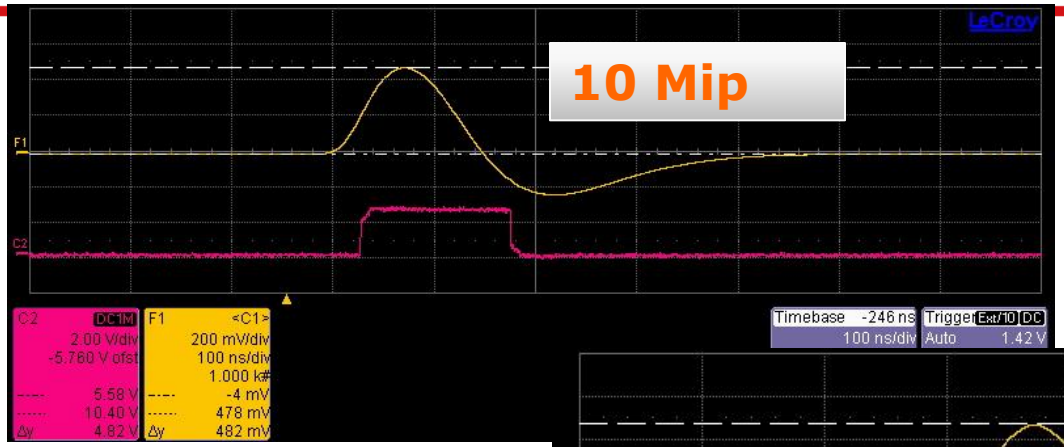
MEASUREMENTS





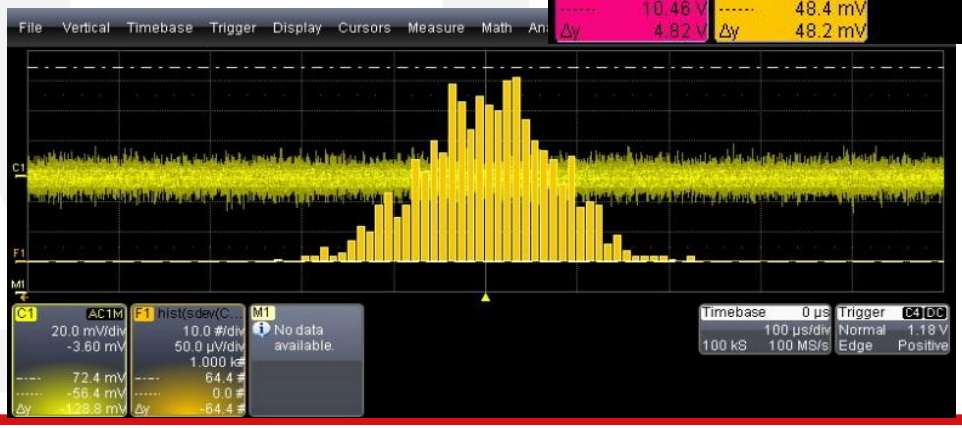
SKIROC2: Fast Shaper noise

Omega



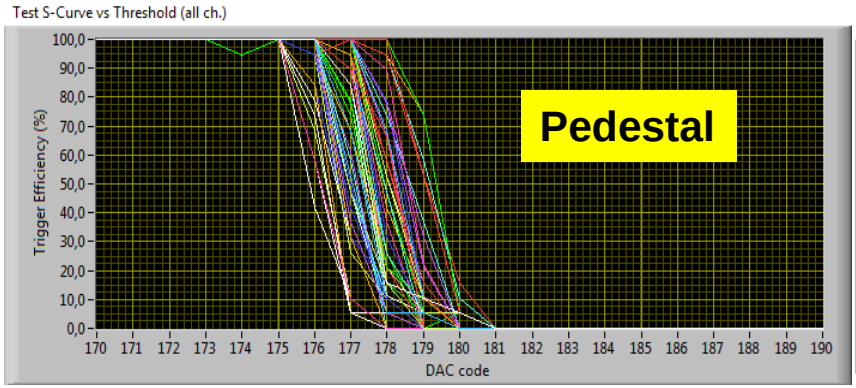
Cdetector ≈ 30 pF

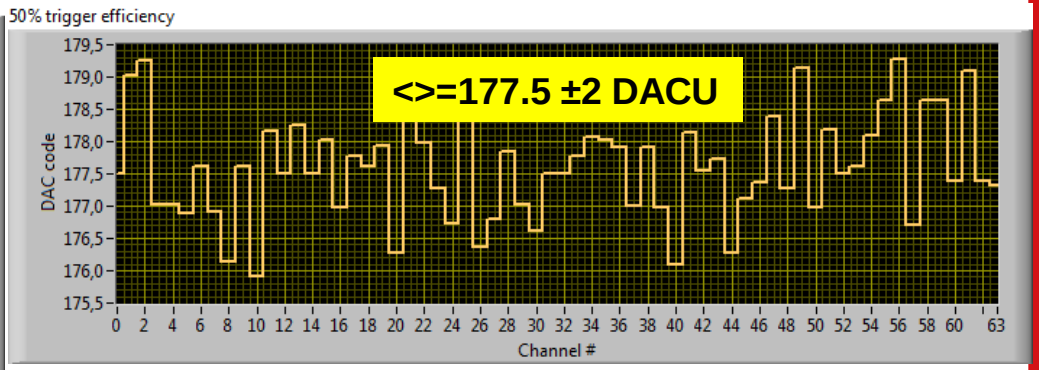
Fast Shaper
~ 50mV/Mip

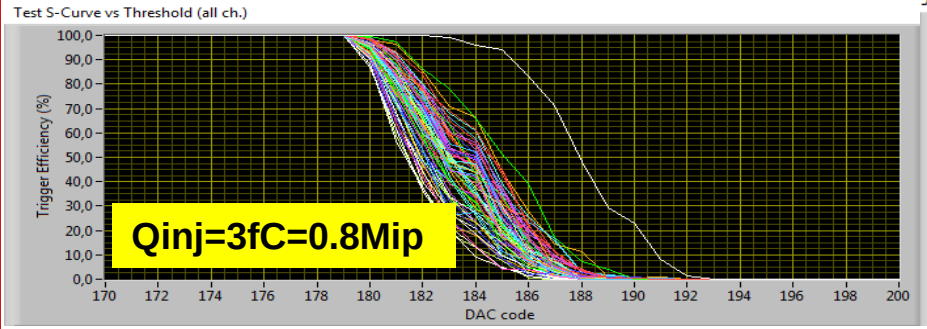


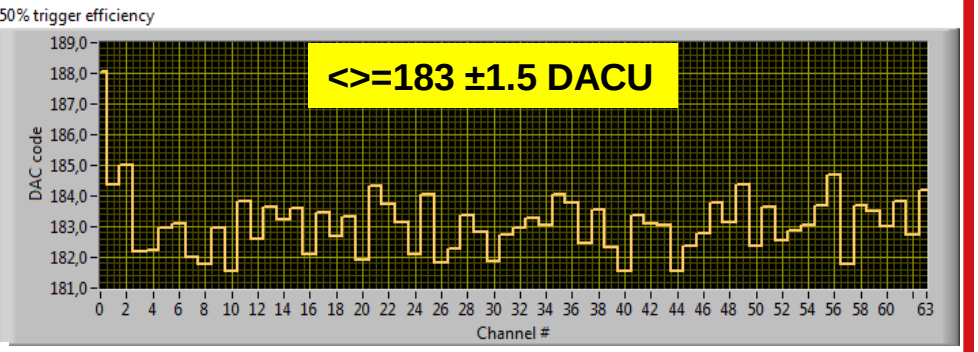
rms noise= 5.3 mV ie 1/10 MIP
S/N=10

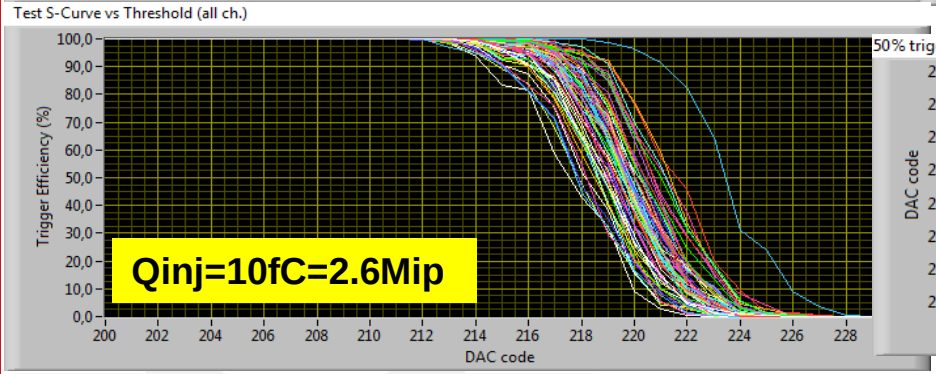
Trigger efficiency (1)

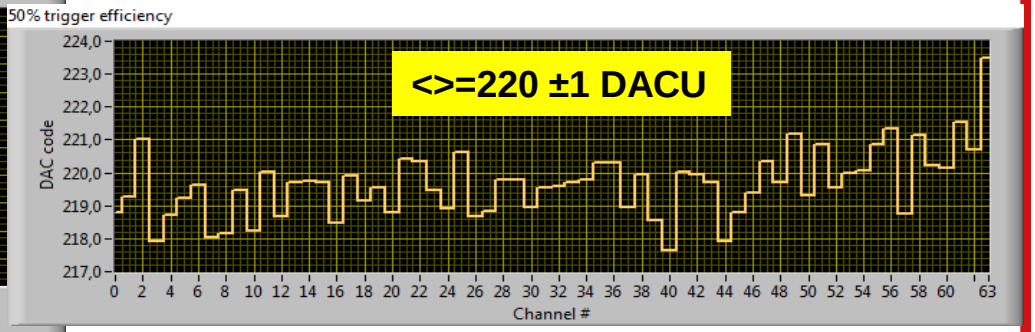




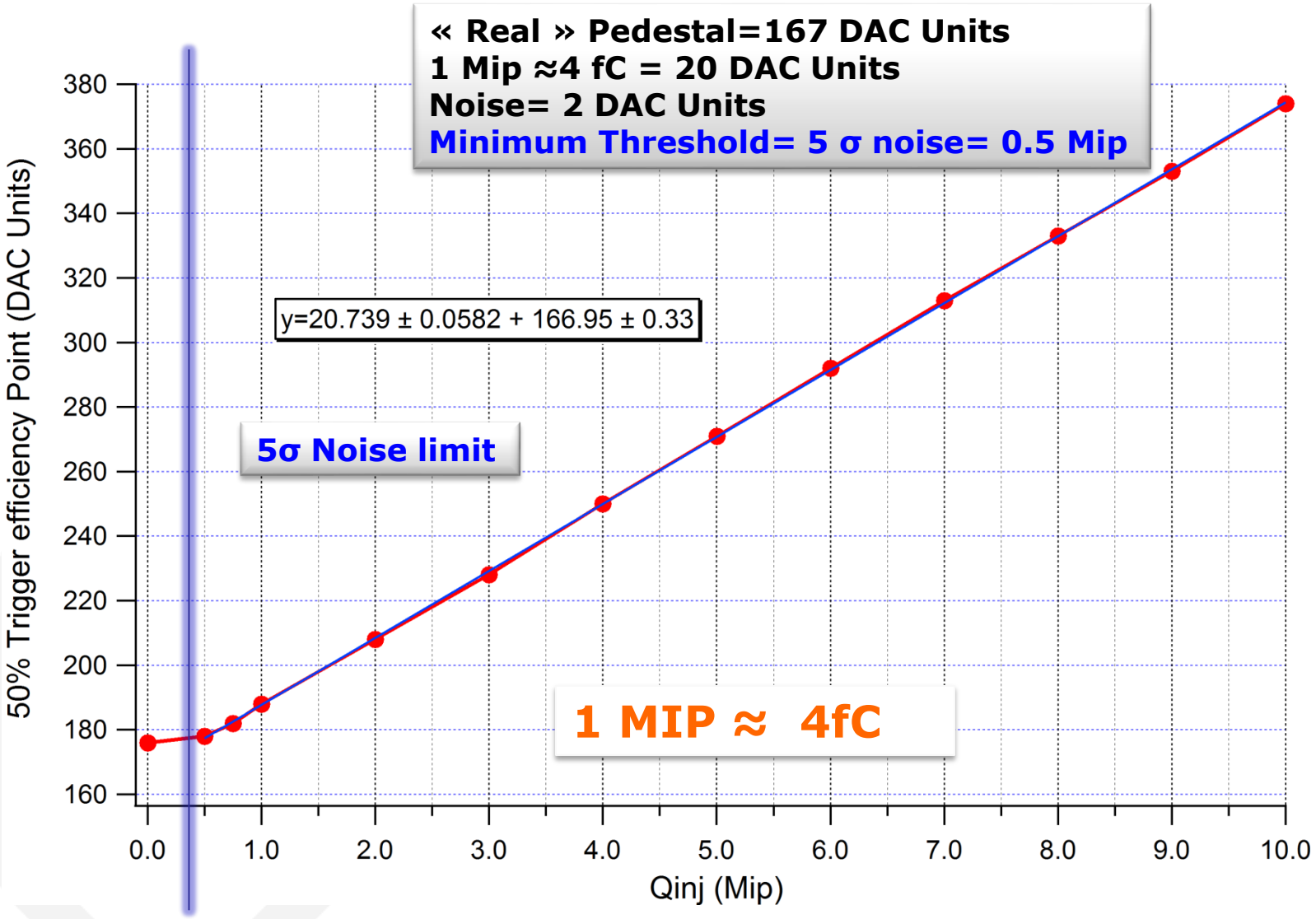




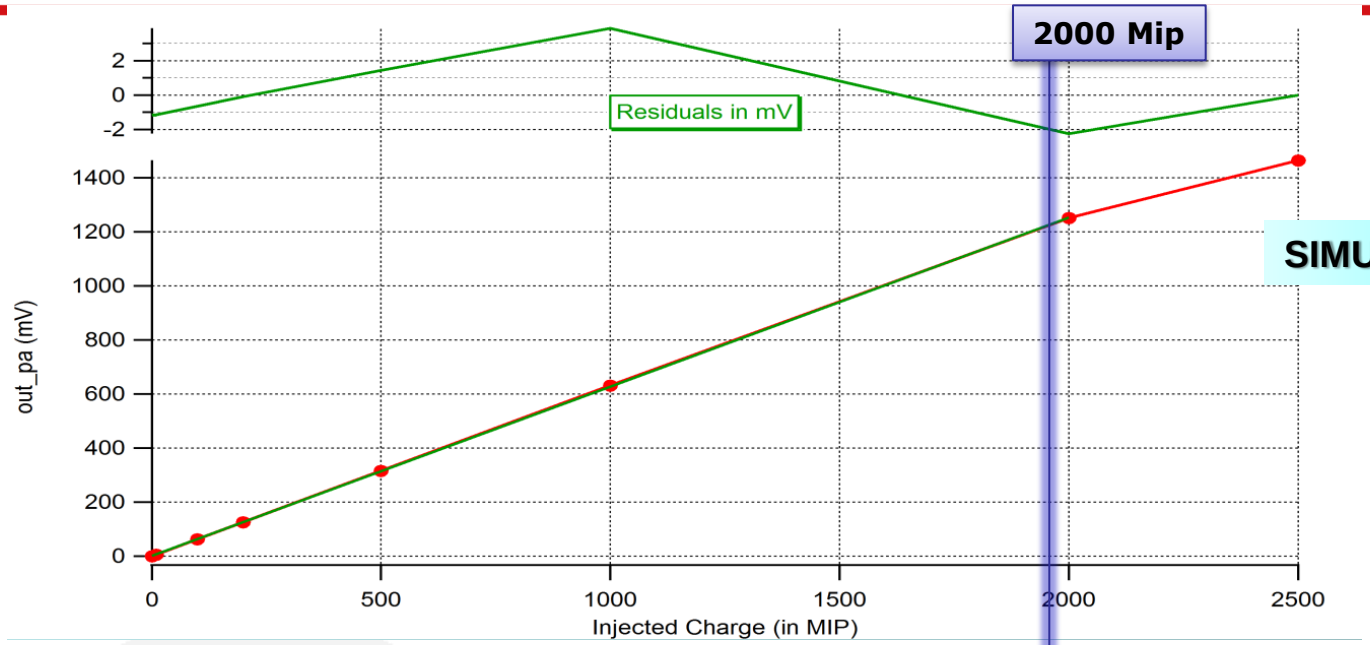




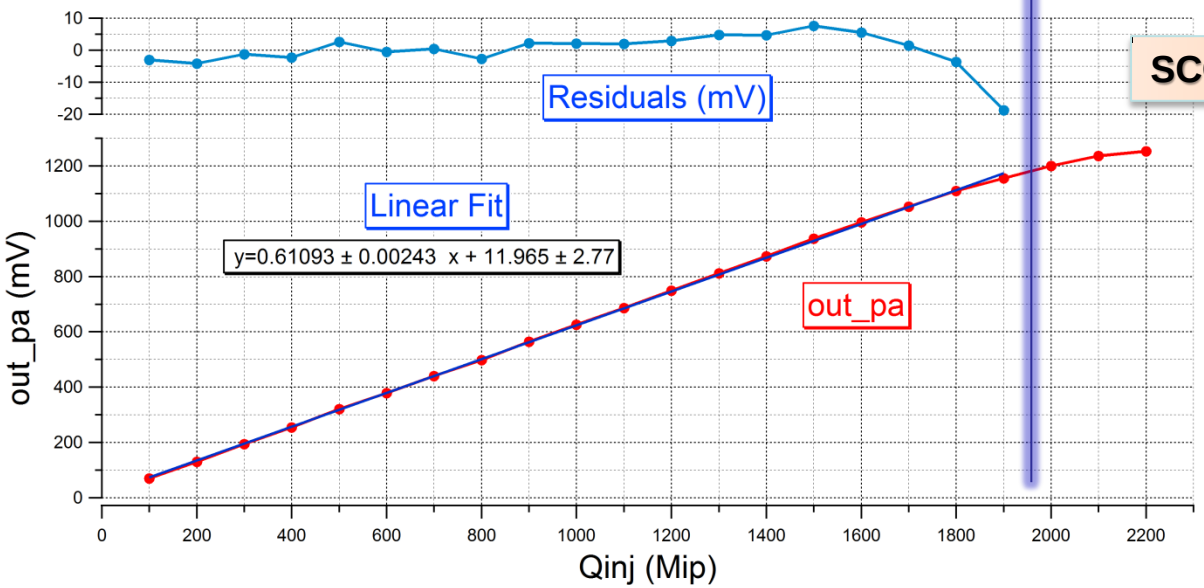
Trigger efficiency (2)



Linearity of the Charge Preamp



SIMULATION

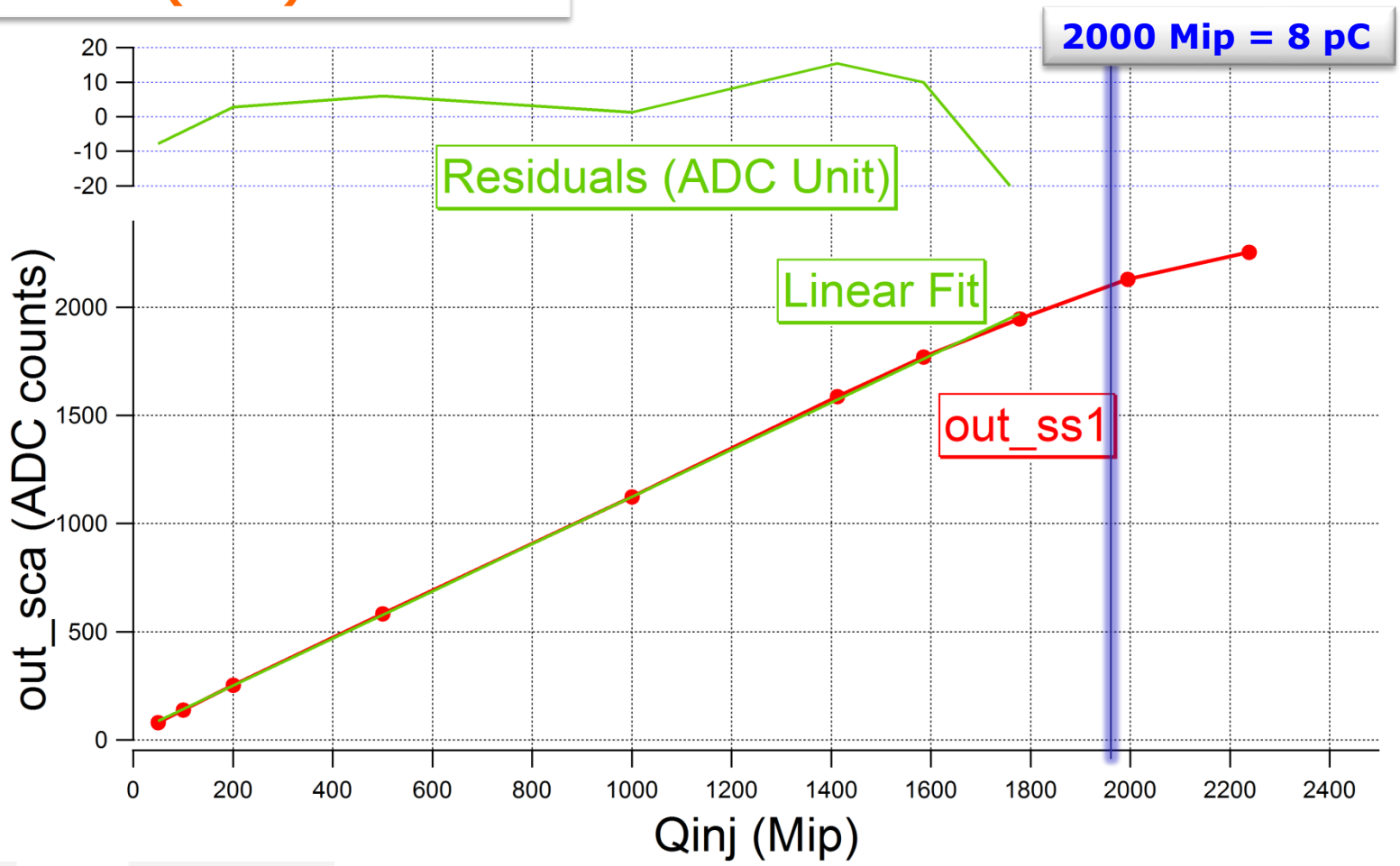


SCOPE MEASUREMENTS

Linearity of the Low Gain Shaper

MEASUREMENTS using SCA and internal ADC

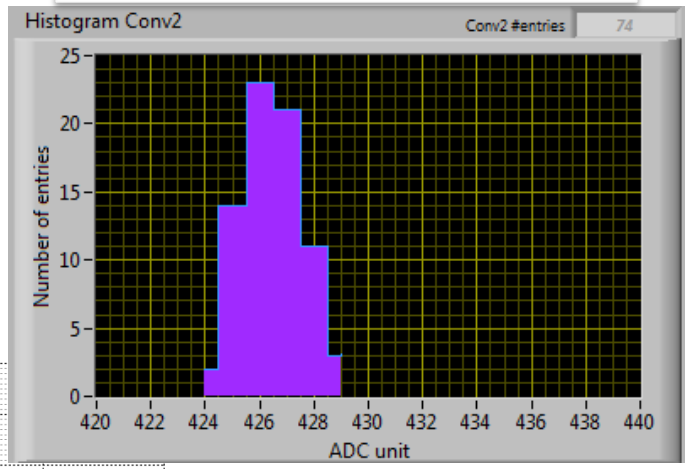
Autotrigger Mode
With 1 MIP (4 fC) threshold



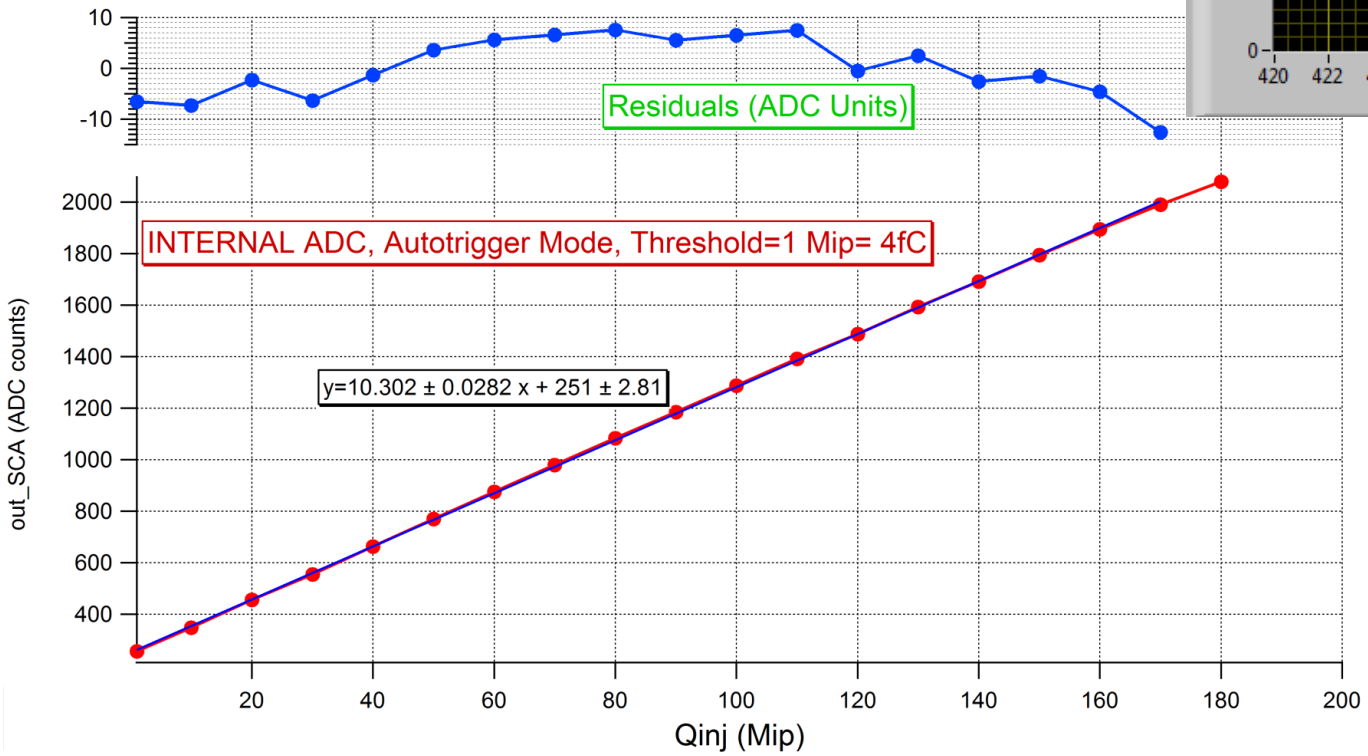
Linearity of High Gain Shaper

Noise = 630 µV
1 Mip gives 5.7 mV
S/N=9

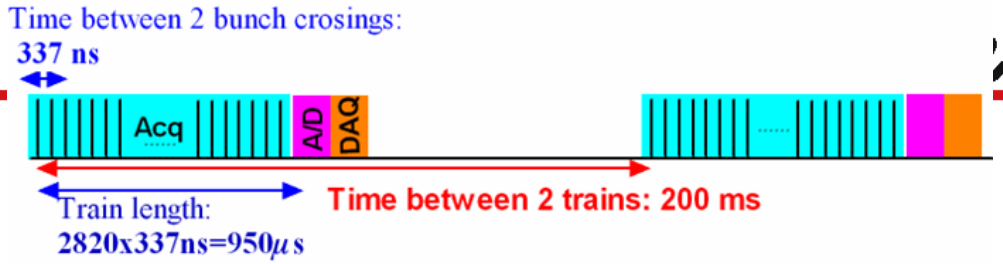
ss10@20 Mip
Rms =1.16 ADC U=600µV



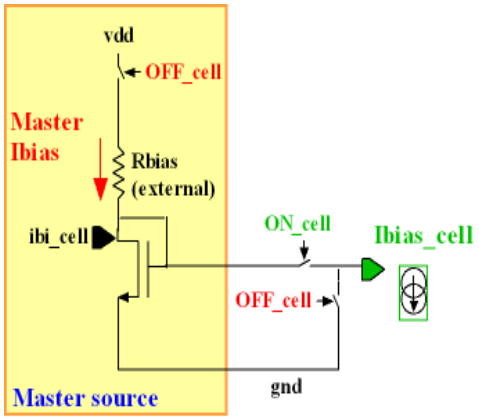
MEASUREMENTS using SCA and internal ADC
Autotrigger mode
1 MIP (4fC) threshold



POWER PULSING



- **Requirement:**
  - **25 μW/ch with 0.5% duty cycle**
  - **500 μA for the entire chip**



- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
- **SK2 power consumption measurement:**
  - 123 mA x 3.3V ≈ 40 mW => **0.6 mW/ch**

- **4 Power pulsing lines** : analog, conversion, dac, digital
- Each chip can be forced **on/off by slow control**

Measurements		
Acquisition	88 mA , 290 mW	Duty Cycle =0.5%, 1.45 mW
Conversion	27.3 mA, 90 mW	Duty Cycle =0.25%, 0.225 mW
Readout	8.0 mA, 26.4 mW	Duty Cycle =0.25%, 0.066 mW

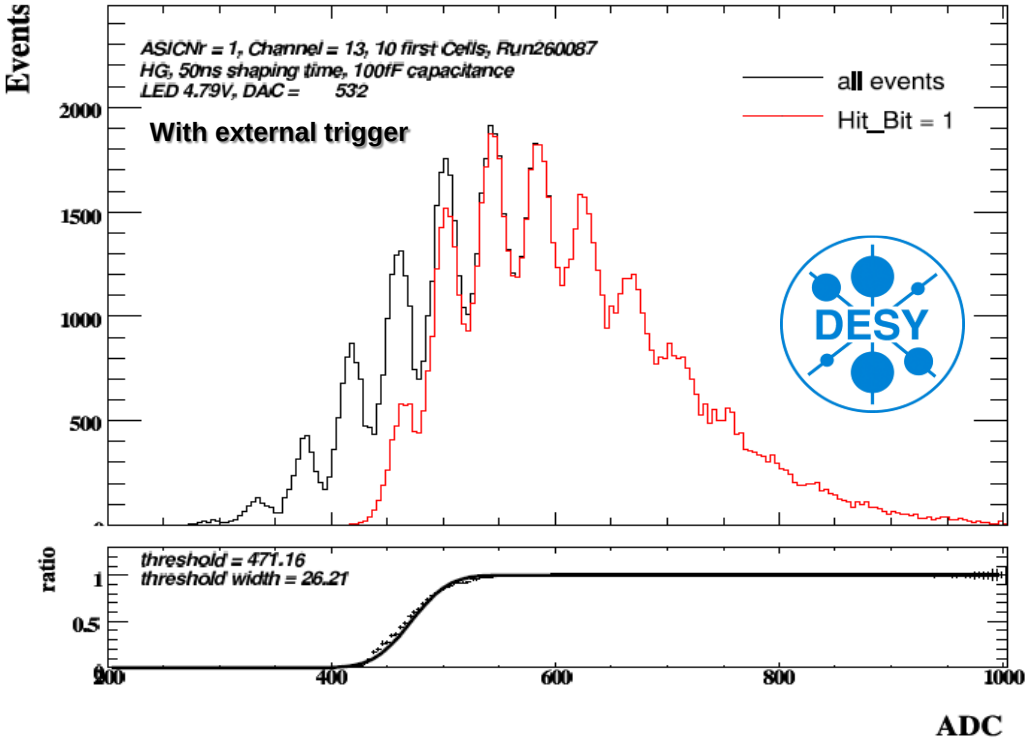
Skiroc2 power consumption with Power pulsing: 1.7 mW ie 27 μW/ch

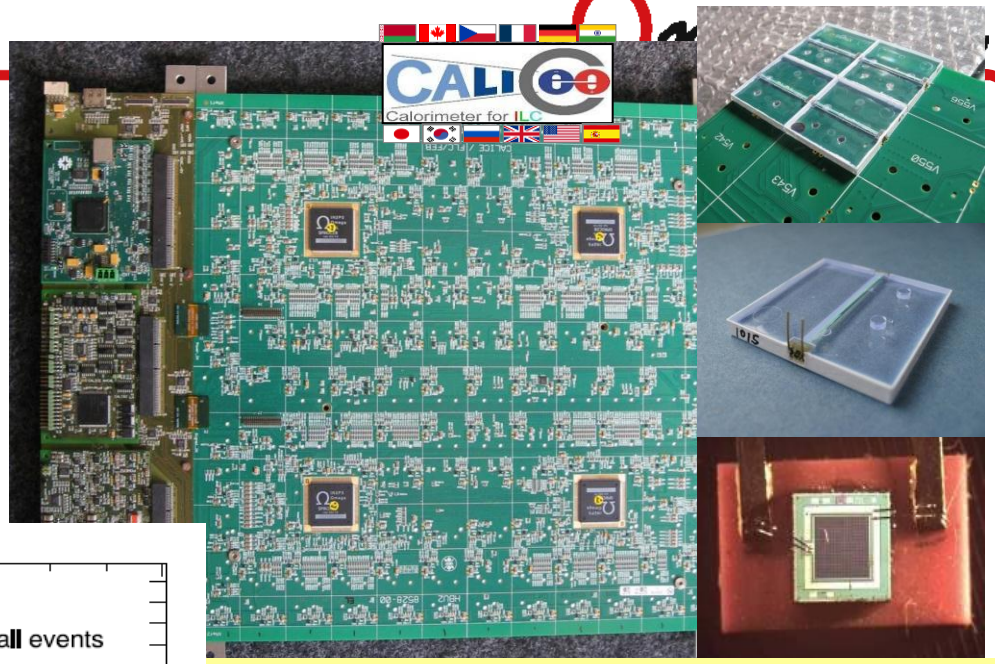
SPIROC2/SKIROC2

- SPIROC2 : Si PM Readout Chip
  - **SIMILAR to SKIROC2**
  - similar dynamic range

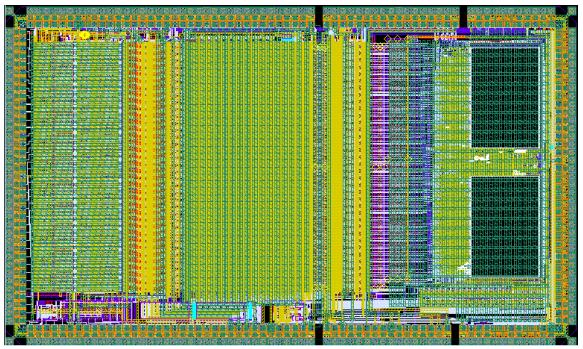
  0.1 pe – 2000 p.e. (1 pe. = 160 fC)
  - All backend similar
  - But different preamplifer, 36 channels

With internal (auto) trigger
And internal ADC



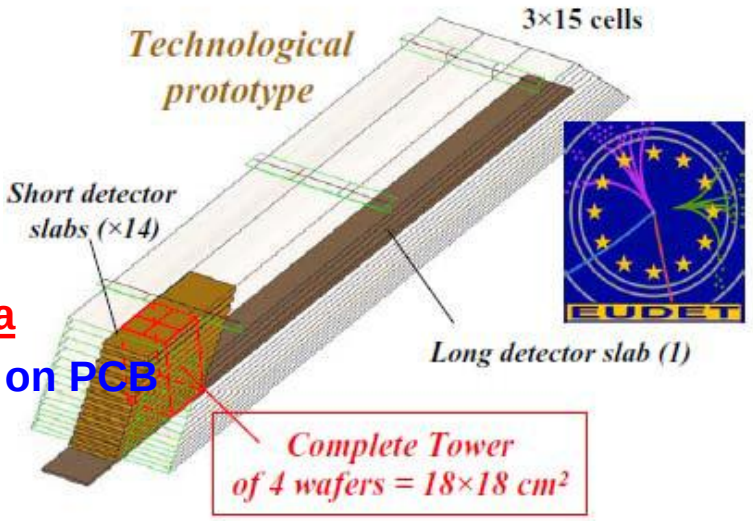


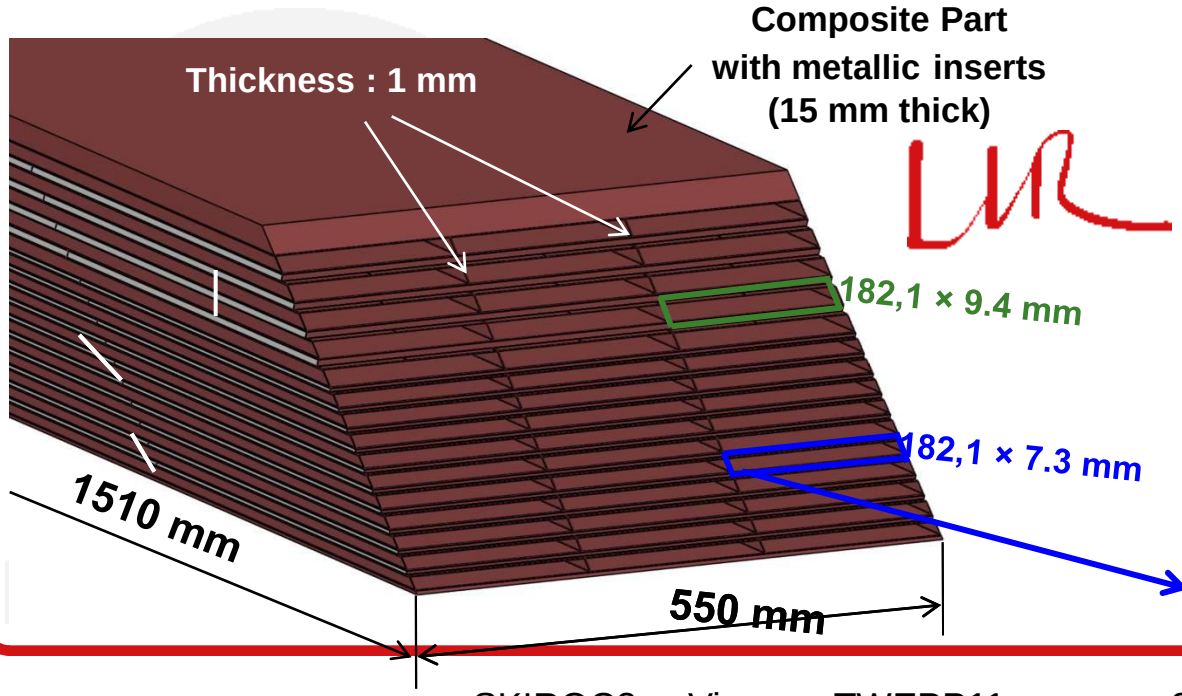
$(0.36m)^2$ Tiles + SiPM + SPIROC (144ch)

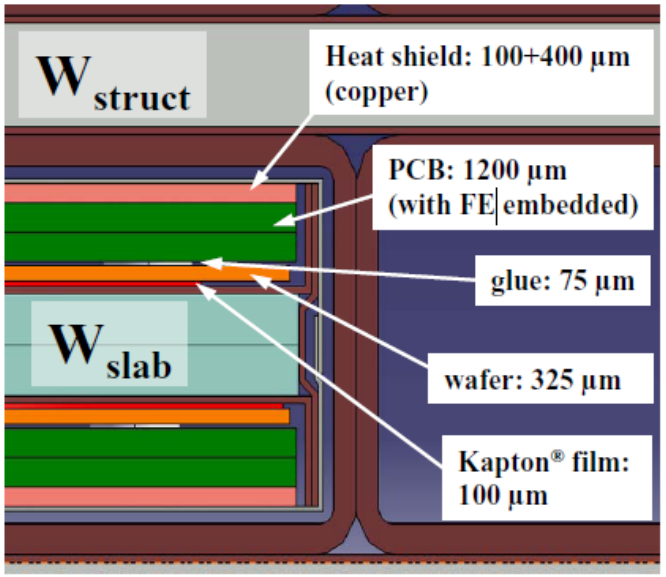


EUDET/AIDA ECAL technological prototype (1)

- Next steps towards a LC detector
- 2/3 final module size (partially equipped)
- 9 cm sensors
- Mechanical housing
  - 15 Tungsten plates wrapped into carbon fibre
  - 7mm thick detector slab slided into the alveola
- 1 tungsten core, 2 layers of detector + electronics on PCB





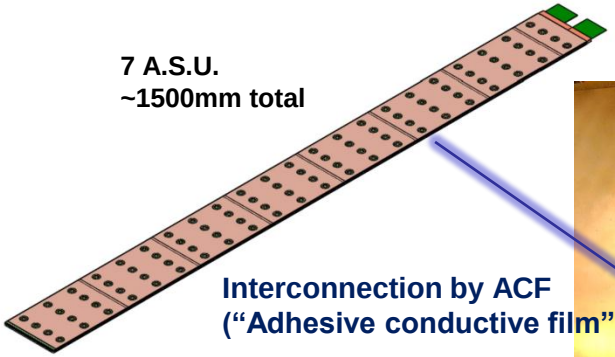


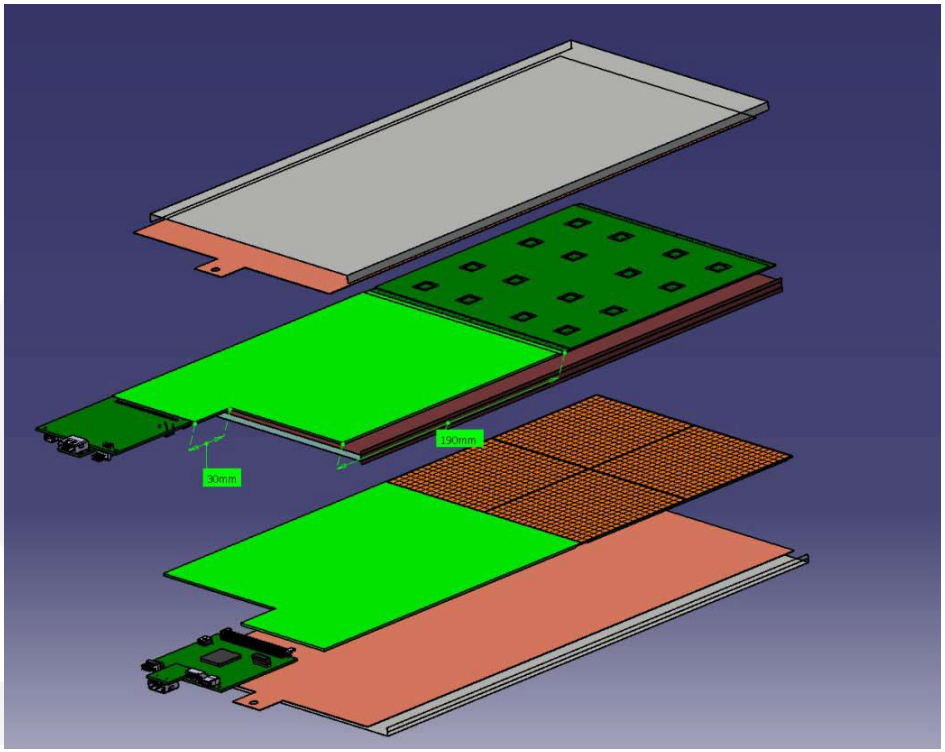
EUDET/AIDA ECAL technological prototype (2)

- In each alveola: 2 layers of 1 to 7 Active Sensors Units (ASU)

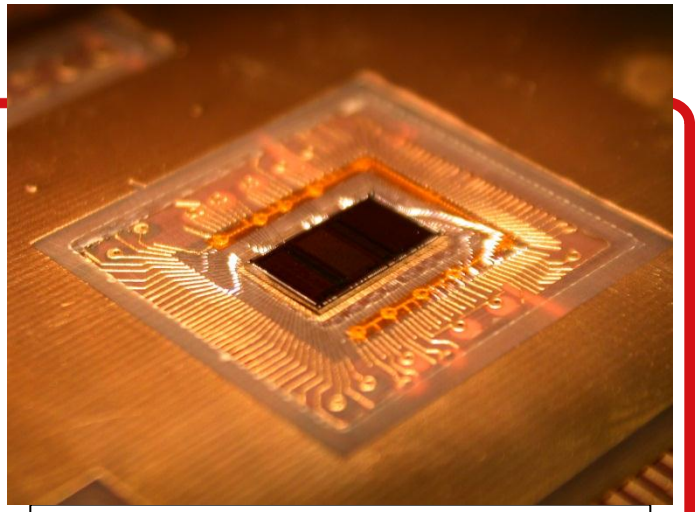
- 1 ASU
  - 1 kapton (HV bias of the PIN diodes)
  - + 1 layer of PIN diodes
  - + 1 PCB with embedded SKIROC2
  - + 1 thermal drain (copper)

@LLR(Palaiseau)



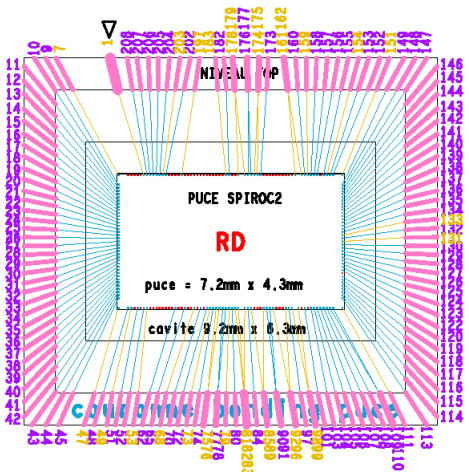


PCB with embedded Chip

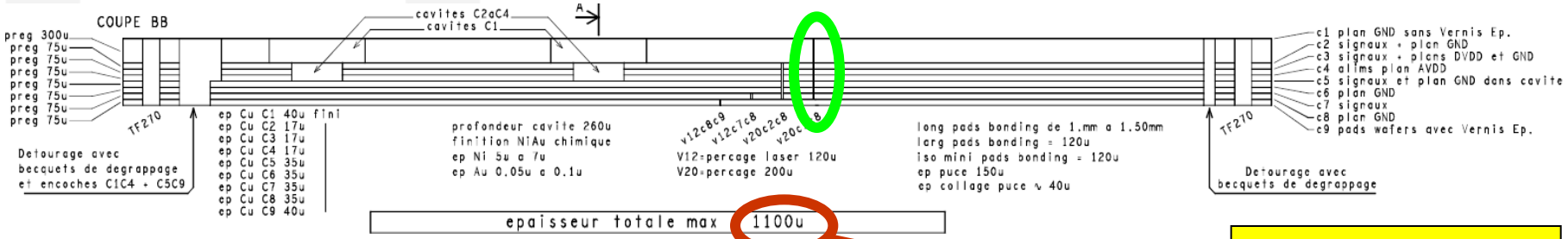


Pile-up	
Top	GND cover layer
C2	GND + Input chip signal
C3	horizontal routing + DVDD + GND
C4	AVDD
C5	GND + vertical routing
C6	GND (pads signal shielding)
C7	pads routing
C8	GND (pads shielding)
BOT	PADS

Front End Board (FEV board)

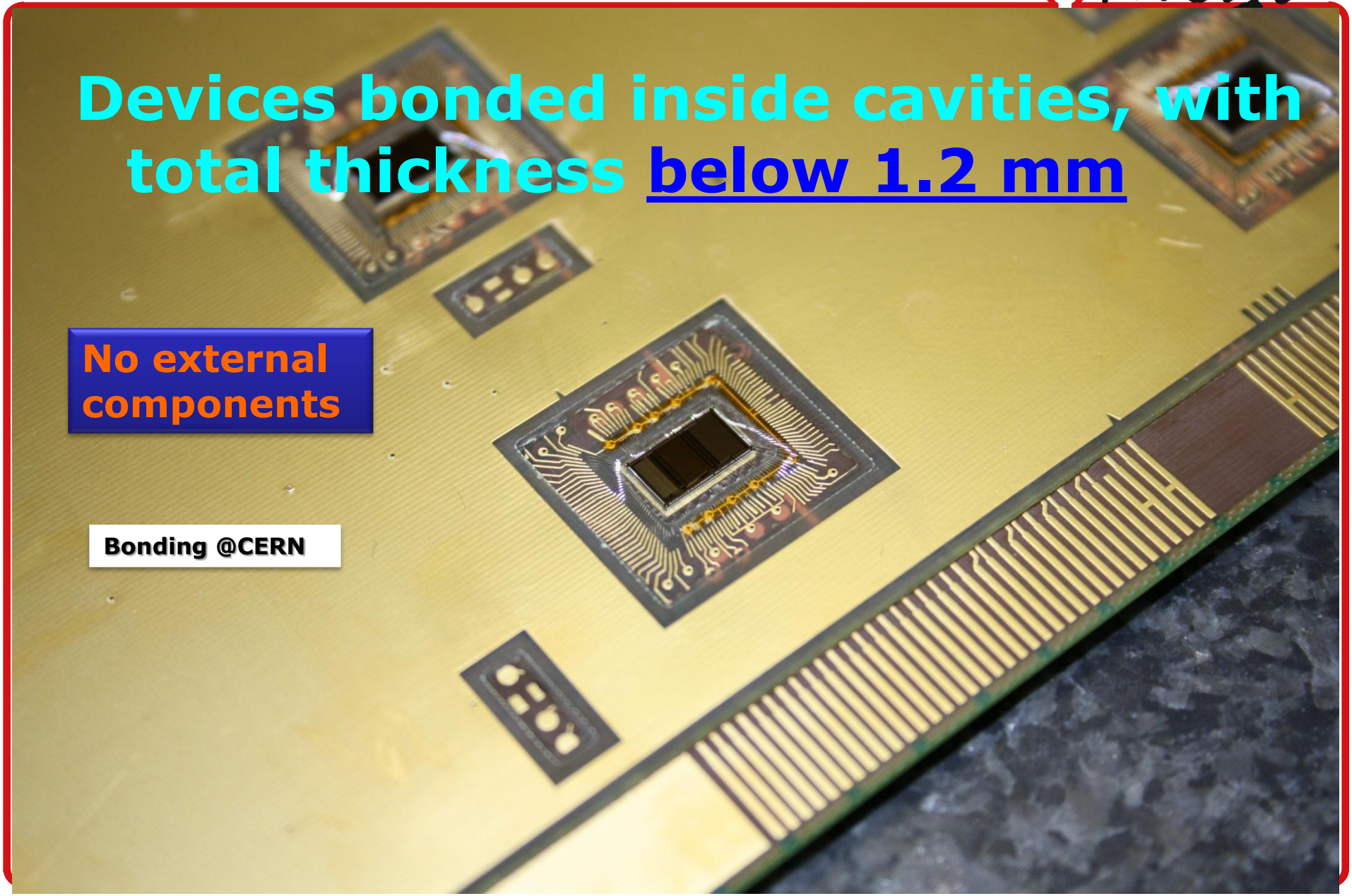


5 drilling sequences :
- Laser C8-C9 120µ filled
- Laser C7-C8 120µ
- Mechanical C2-C8 200µ
- Mechanical C1-C8 200µ
- Mechanical C1-C9 (for PCB fastening)



PCB Thickness 1100 µm

FEV board

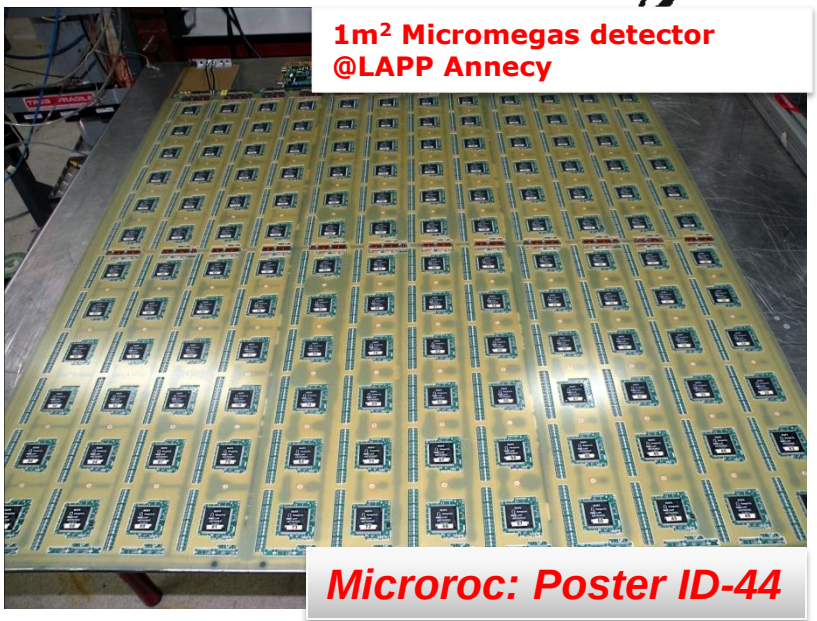

Devices bonded inside cavities, with total thickness below 1.2 mm
No external components
Bonding @CERN

CONCLUSION

- Good performance of SKIROC2:
  - 0.5 Mip (2 fC) up to 2000 Mip (8 pC) dynamic range
  - 0.1Mip noise (0.4 fC ie 2500 electrons), minimum threshold 0.5 Mip, autotrigger mode
- Many fine measurements to be continued
- Test with FEV and sensors to be done at system level (power pulsing, DAQ)

DAQ: Poster ID-109

- 3rd generation of ROC chips to be done 2012-2013 within the AIDA program.

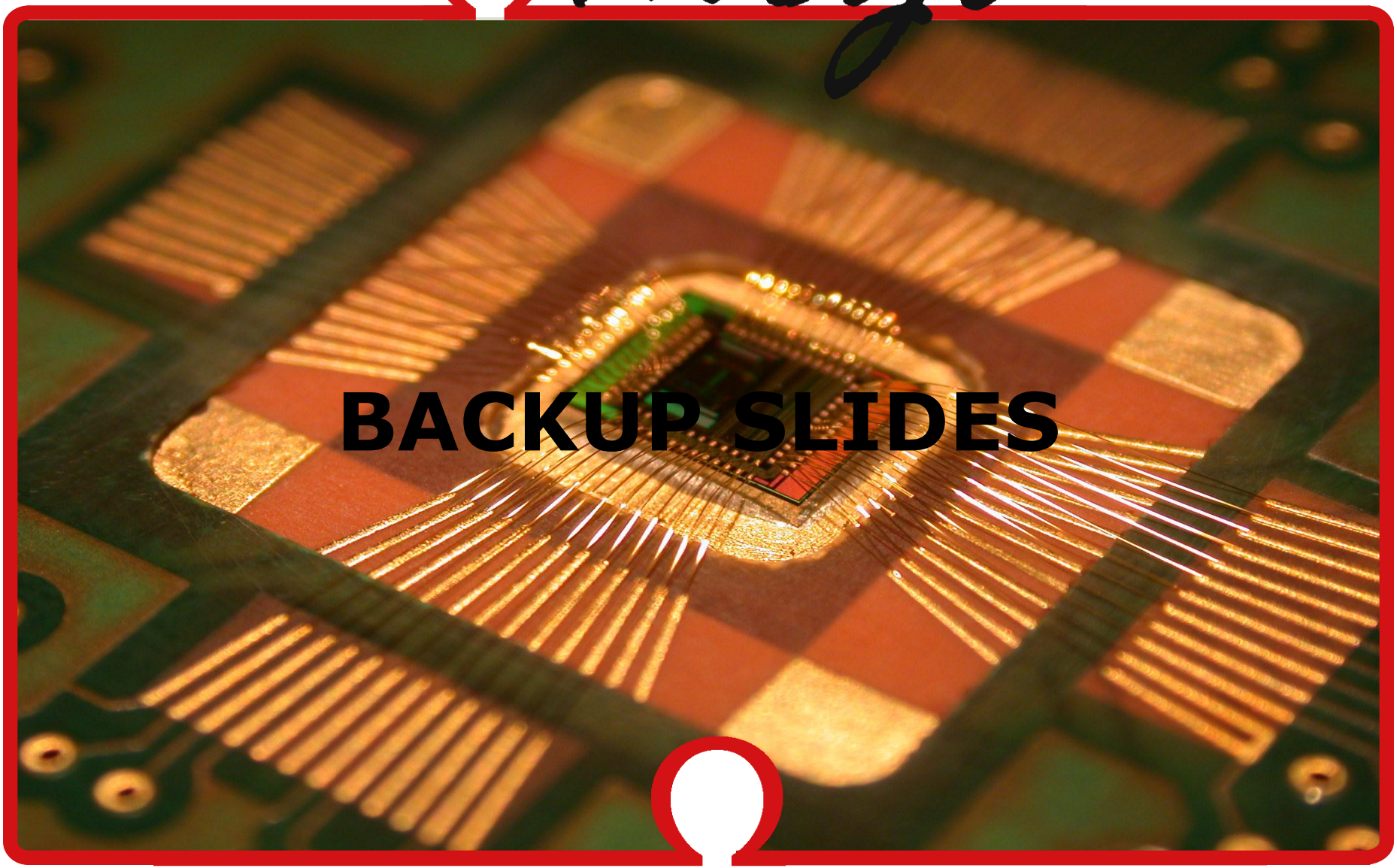


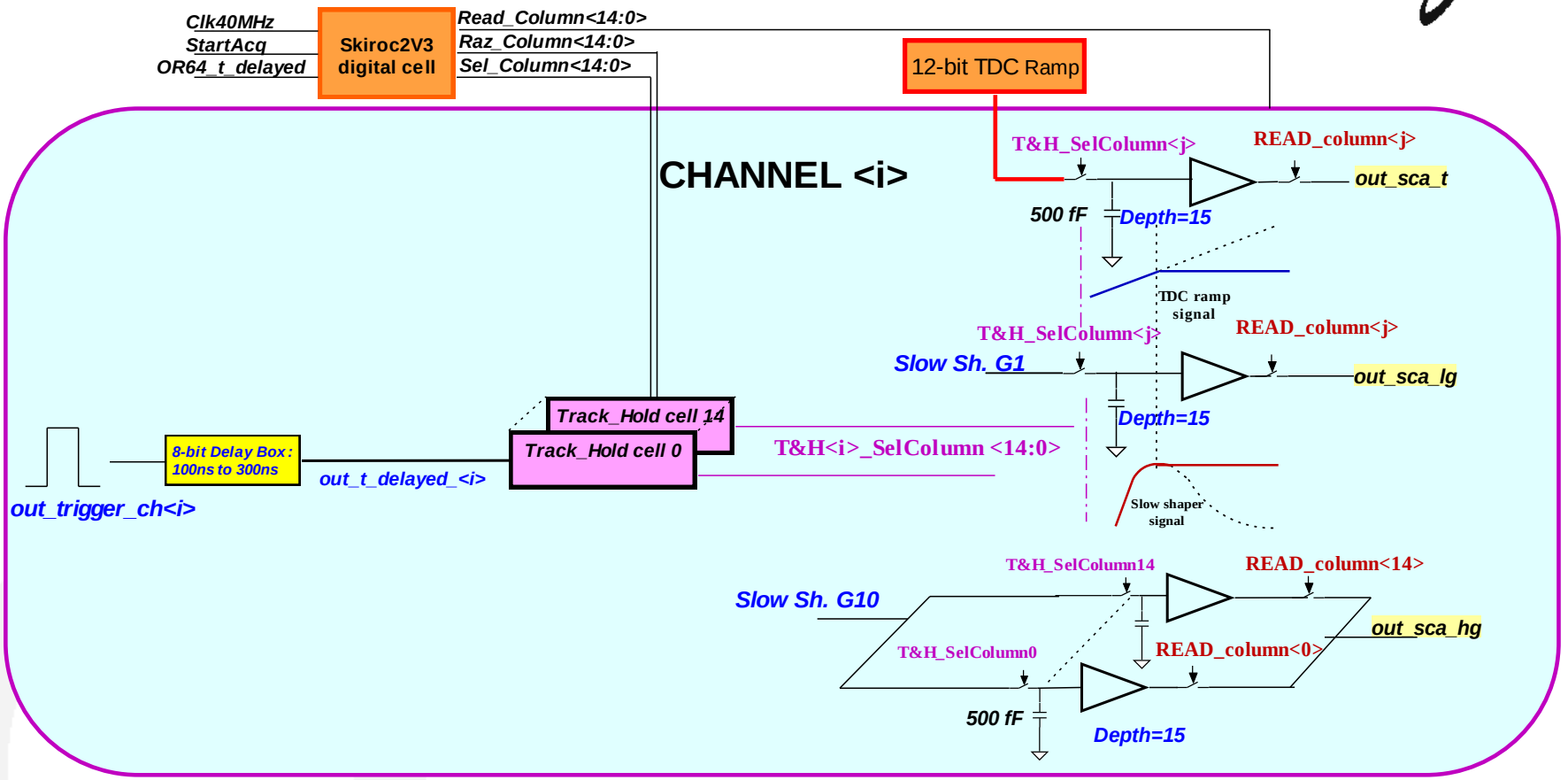
1m² Micromegas detector @LAPP Annecy

Microroc: Poster ID-44

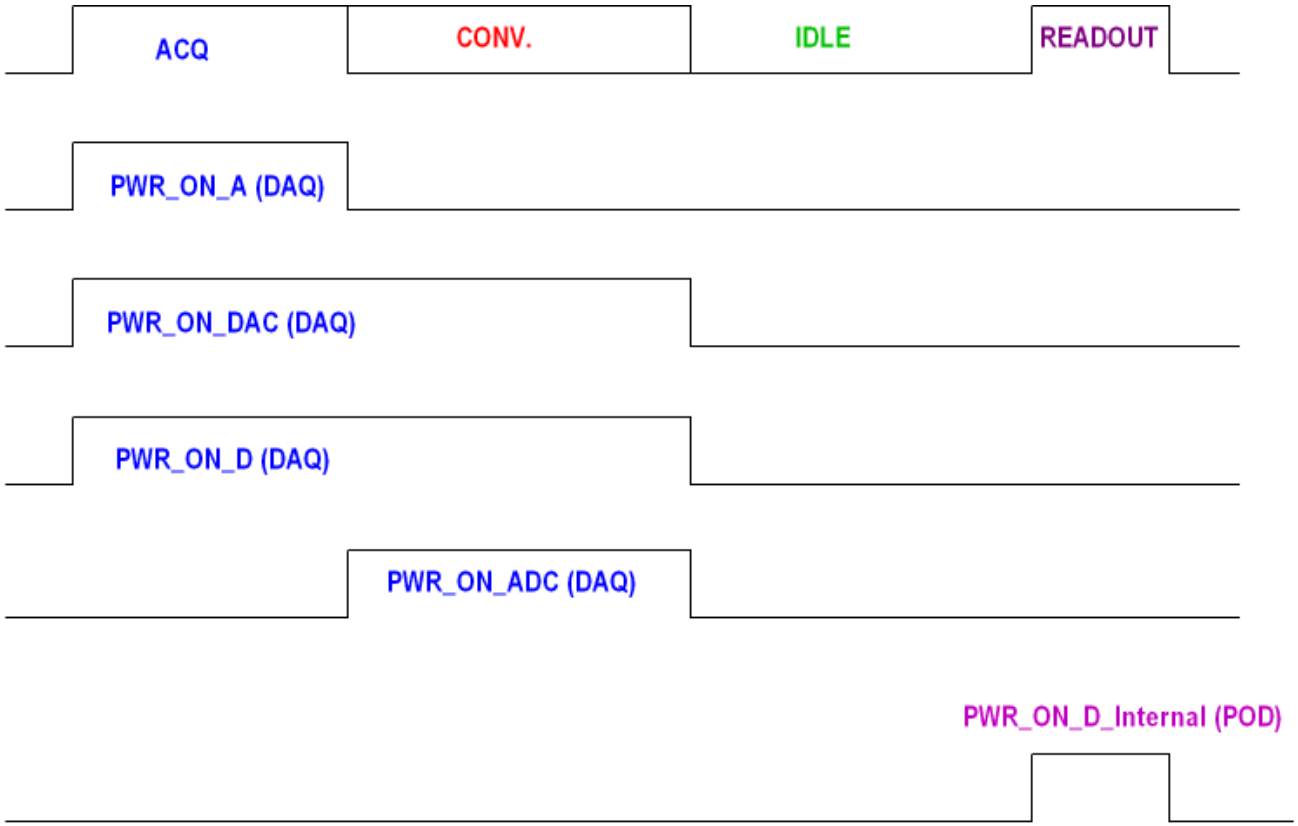
@IPNL Lyon

1 m³ RPC detector, 40 layers
Hardroc2: 37 000 channels


BACKUP SLIDES


Clk40MHz
StartAcq
OR64_t_delayed
Skiroc2V3 digital cell
Read_Column<14:0>
Raz_Column<14:0>
Sel_Column<14:0>
12-bit TDC Ramp
CHANNEL <i>
T&H_SelColumn<j>
READ_column<j>
out_sca_t
500 fF
Depth=15
TDC ramp signal
T&H_SelColumn<j>
READ_column<j>
Slow Sh. G1
out_sca_lg
Depth=15
Track_Hold cell 14
Track_Hold cell 0
T&H<i>_SelColumn <14:0>
8-bit Delay Box : 100ns to 300ns
out_t_delayed_<i>
out_trigger_ch<i>
Slow shaper signal
T&H_SelColumn14
READ_column<14>
Slow Sh. G10
out_sca_hg
T&H_SelColumn0
READ_column<0>
500 fF
Depth=15

Power pulsing lines timing



CONVERSION:

HARDROC2: NO conversion

SPIROC2: max time (Full chip)= 16 SCAx 2 (HG or LG/Time) x103 µs=3.2ms

SKIROC2: max time (Full chip)= 15 SCA x2 (HG or LG/Time) x103 µs= 3 ms

READOUT:

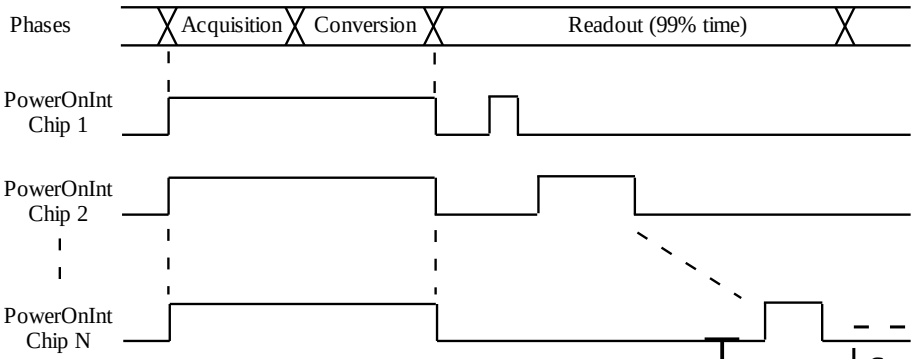
HARDROC2: 127 (memory depth)x [64 channelsx 2 trigger bits + 24 BCID bits + 8 Header bits]=20 320 bits => 200 nsx20k=4 ms/ Full Chip (WORST case)

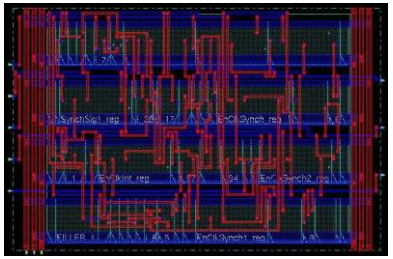
SPIROC2: 16 SCAx2 (HG or LG/Time) x 36 ch x 16 ADC bits + 16 SCAx16 BCID bits + 16 Header bits= 18 704 bits => 3.8 ms/Full Chip (Worst case)

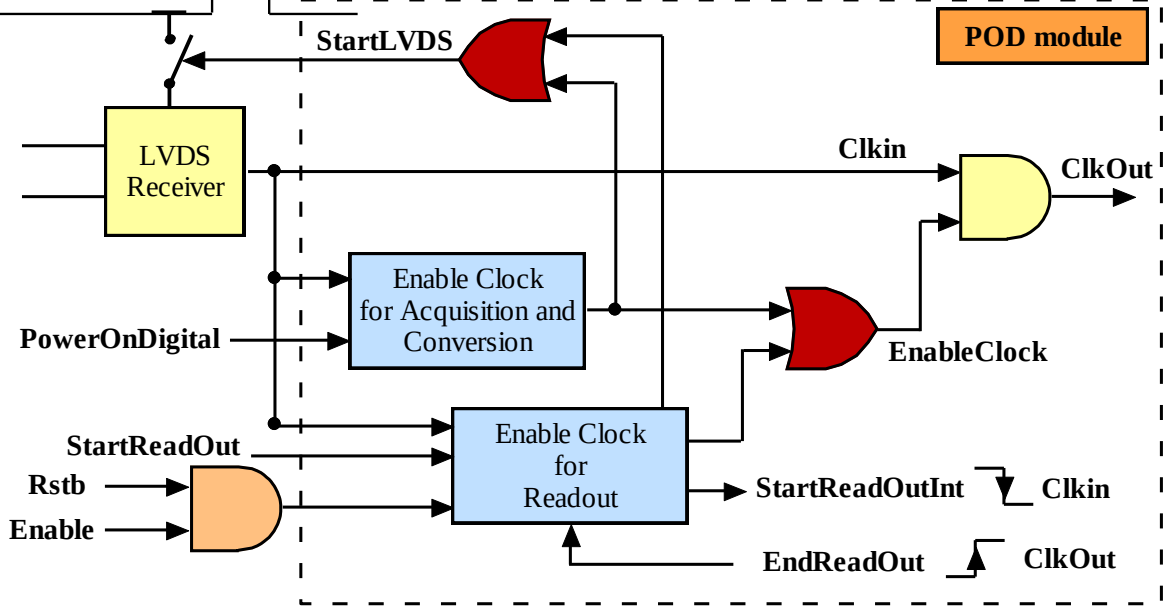
SKIROC2: 15 SCAx2 (HG or LG/Time) x 64 ch x 16 ADC bits + 15 SCAx16 BCID bits + 16 Header bits= 30 976 bits => 6 ms/Full Fhip (Worst case)

Power On Digital Module: POD

- POD module ("Clock-gating") to handle for the 2 LVDS receivers clock (40 MHz and 5 Mhz) and save power:
  - Starts and stops the Clocks, switches OFF LVDS receivers bias currents



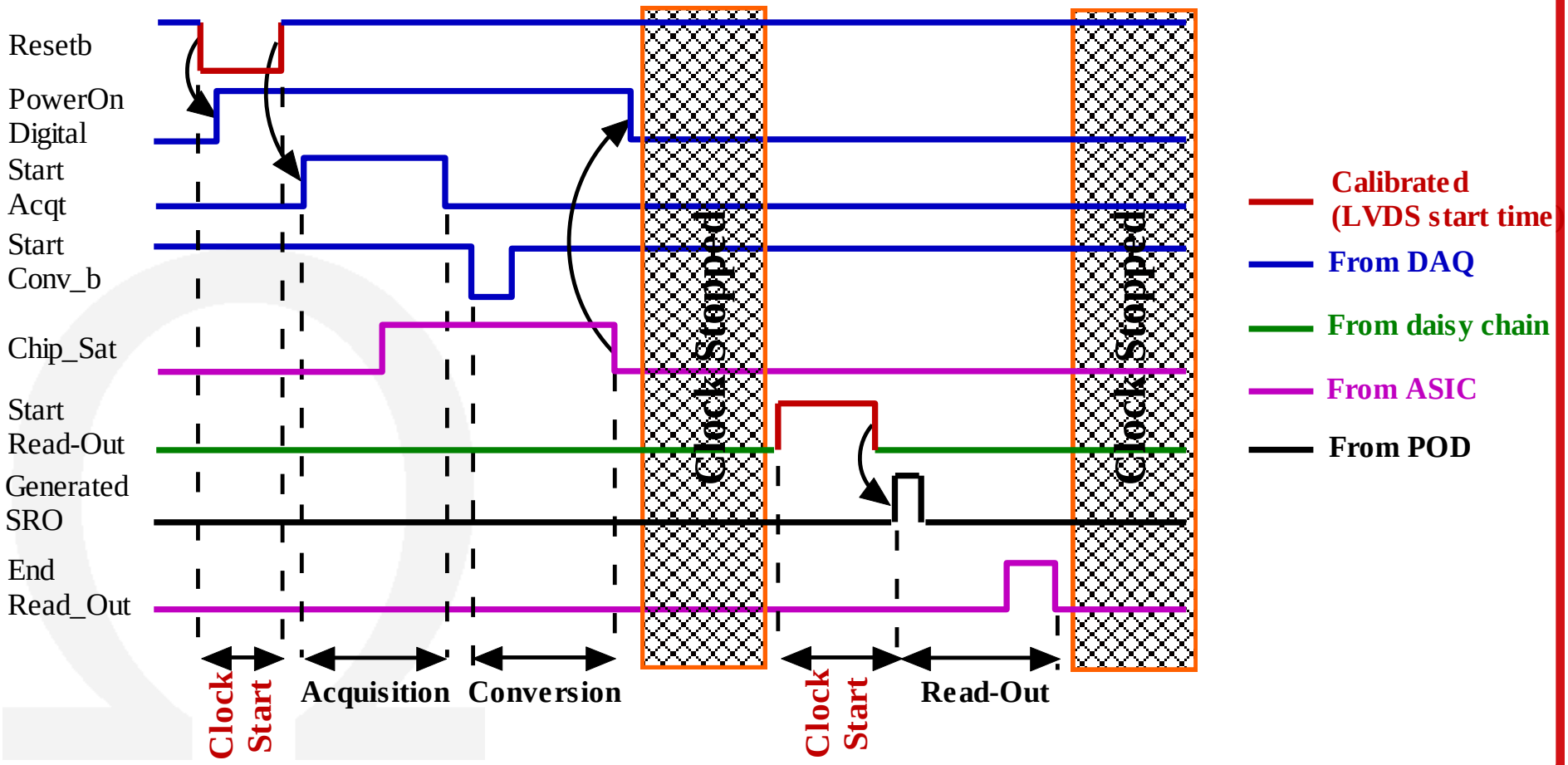




2 others LVDS receivers (RazChn/NoTrig and ValEvt) active during PowerOnAnalog (during bunch crossing)

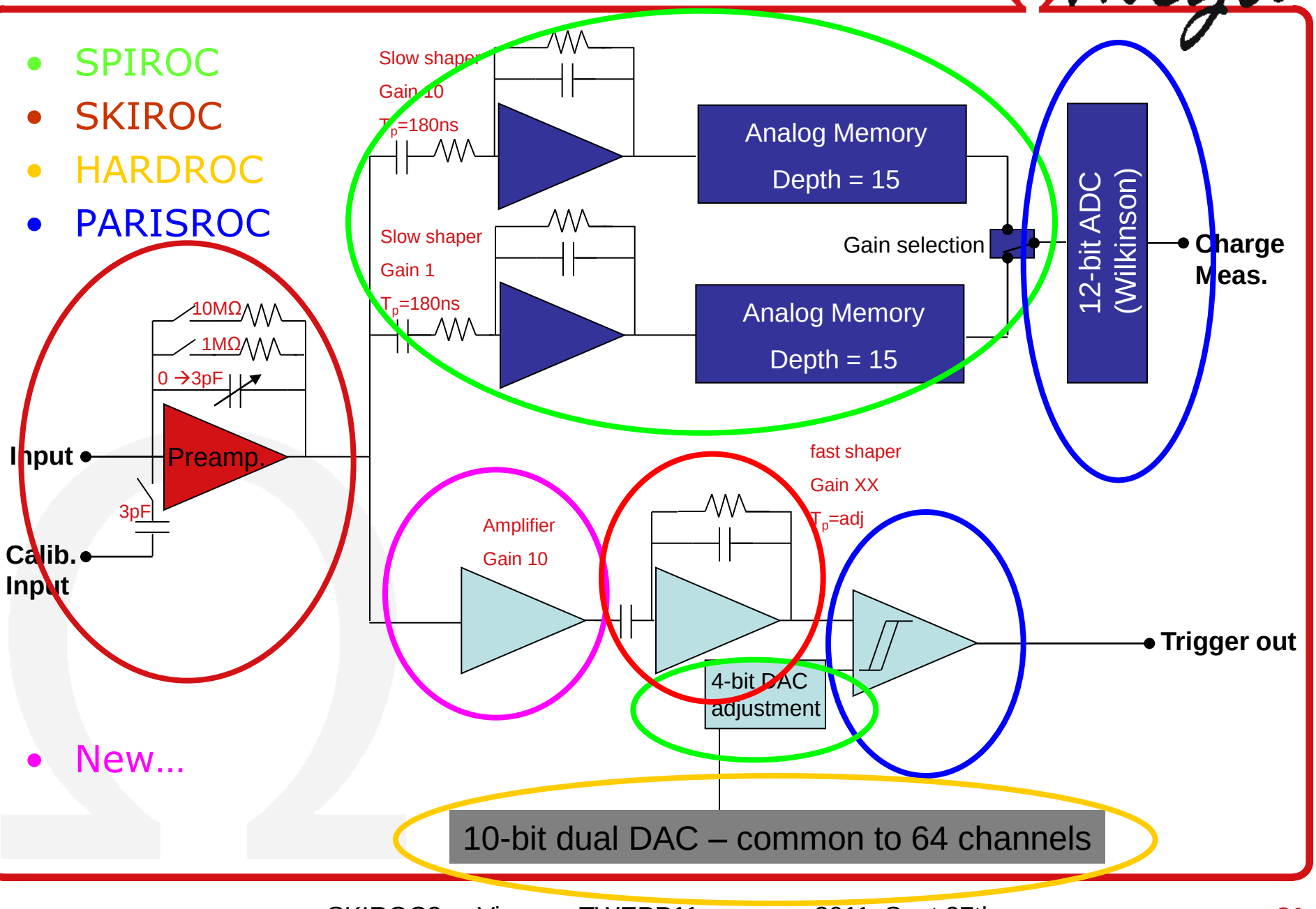
Power On Digital Sequence

- **End of Conversion**: clock stopped as not needed and LVDS receivers bias switched OFF
- **Readout**: Start ReadOut signal generated by the POD and stands for a PwrOnD => starts LVDS receivers and Clk.
- **End of the ReadOut**: The chip generates a EndRout signal which will be used by the next chip in the daisy chain to be read out.



SKIROC2 One channel block scheme

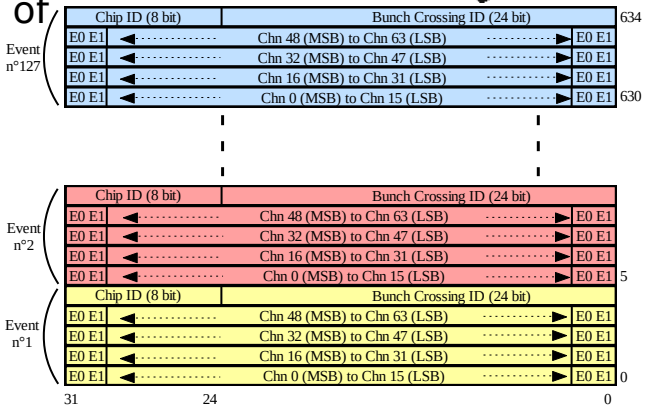
- SPIROC
- SKIROC
- HARDROC
- PARISROC



- New...

MEMORY MAPPING of the ROC CHIPs

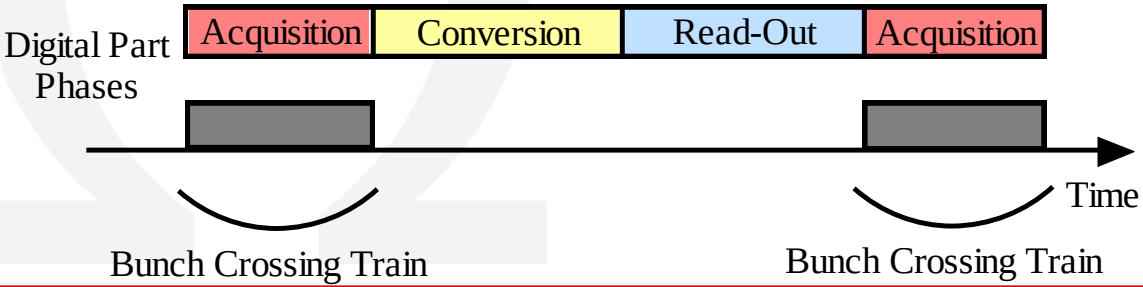
- HARDROC2: 127 events on 2 bits for 64 channels. Maximum of stored data is 20320 bits
  - No conversion
  - Readout worst case: 200 nsx20k=4 ms/ Full Chip (WORST case)

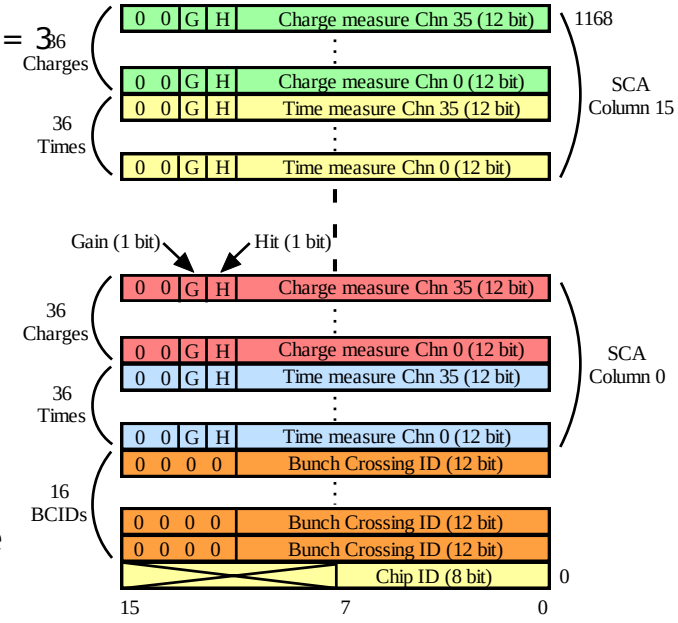


- SPIROC2: 16 events, 36 channels. 12 bits ADC for time and charge => max stored data= 18707 bits
  - Conv.: max time (Full chip)= 16 SCA x 2 (HG or LG/Time) x103 µs=3.2ms
  - RO: 3.8 ms/Full Chip (Worst case)

- SKIROC2: 15 events, 64 channels. 12 bits ADC for time and charge => max stored data= 30976 bits
  - Conv.: max time (Full chip)= 15 SCA x2 (HG or LG/Time) x103 µs= 3 ms
  - ReadOut: 6 ms/Full Fhip (Worst case)

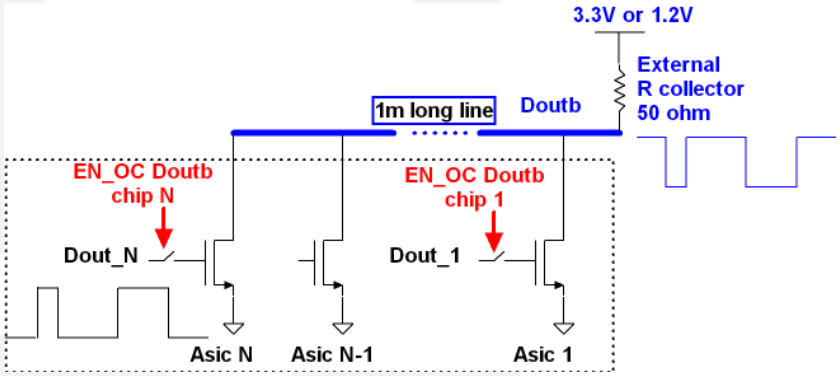
Physics simulation: 2 or 3 SCA are enough

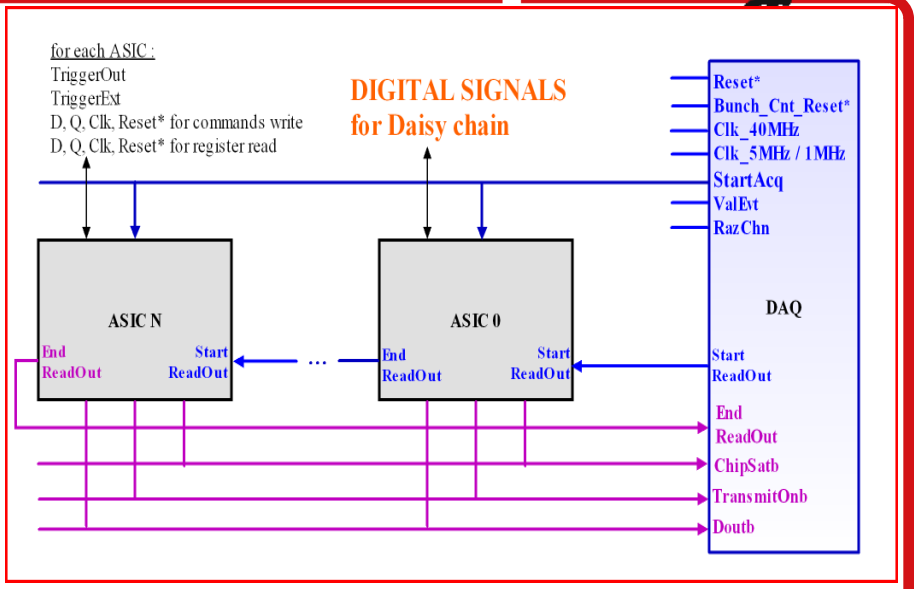




DAISY CHAIN: Main signals

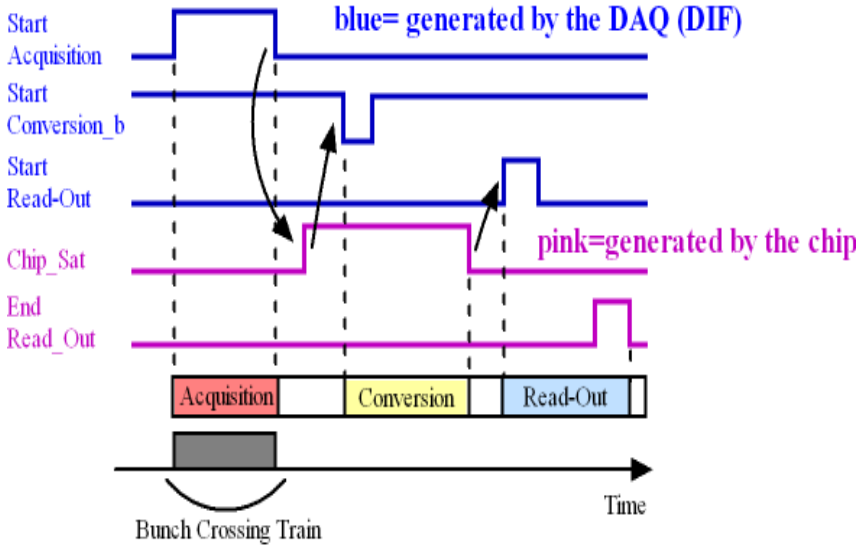
- **COMMON to all the ROC chips**
  - **StartAcq**
    - Start acquisition, generated by DAQ
  - **StartReadout:**
    - Generated by DAQ, start of the readout
  - **EndReadout**
    - Generated by chip, End of the readout
  - **ChipSat** (**O**pen **C**ollector signal):
    - Generated by chip, « 1 »: digital memory is full or acq finished
  - **Dout:** data out (OC signal)
  - **TransmitOn** (OC signal)
    - Generated by chip, Data out are transmitted
- Buffers integrated for OC signals





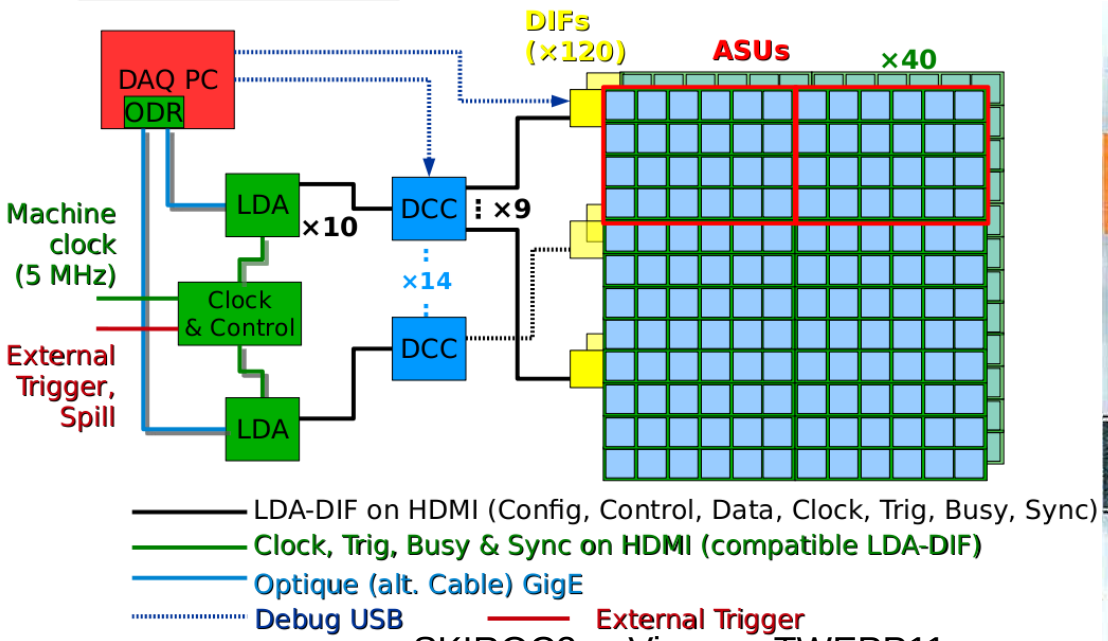
ILC

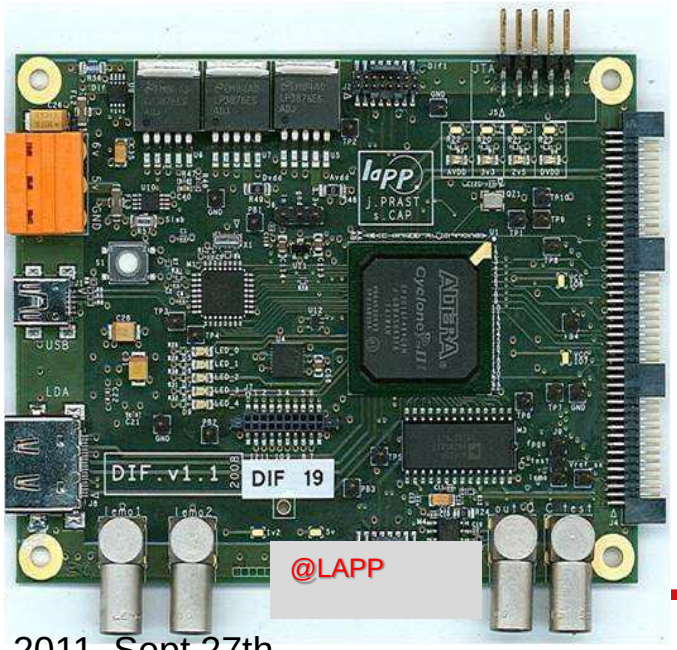
No conversion in Hardroc



INTERFACE DAQ-ROC= DIF board

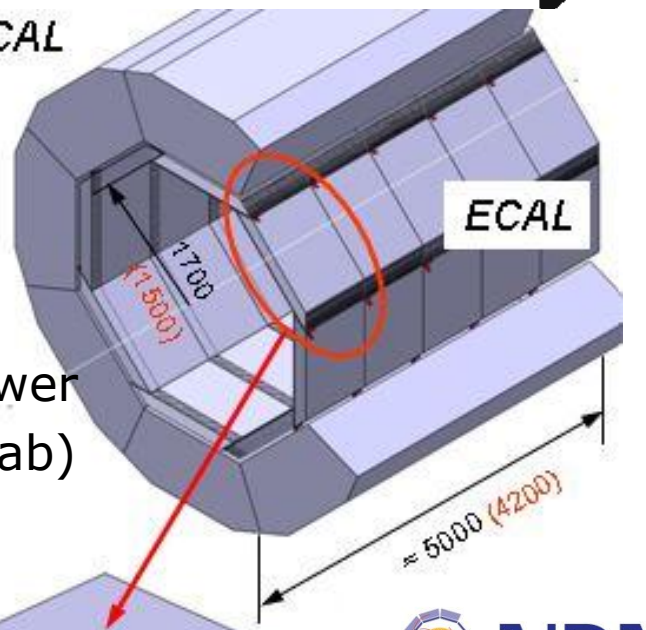
- Reception of the Slow Control parameters from a PC and transmission to the ASICs, launch acquisition, perform analog/digital readout and send all the data received from ASICs to a PC.
- Communication
  - with other DIFs
  - with DAQ either by USB or by HDMI
- The DIF should be able to handle more than 100 ASICs theoretically. The max which has been tested is 48
- **Regulators + Decoupling capacitors located on the DIF**

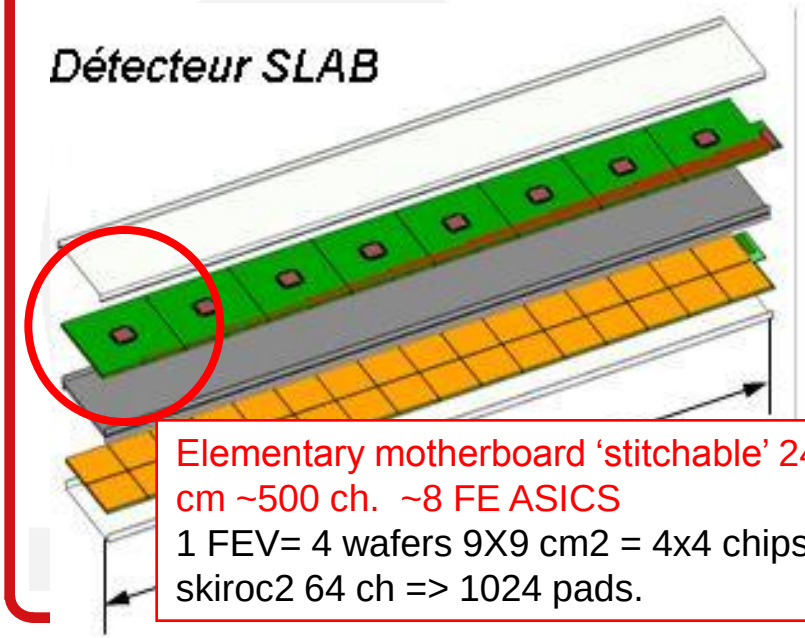


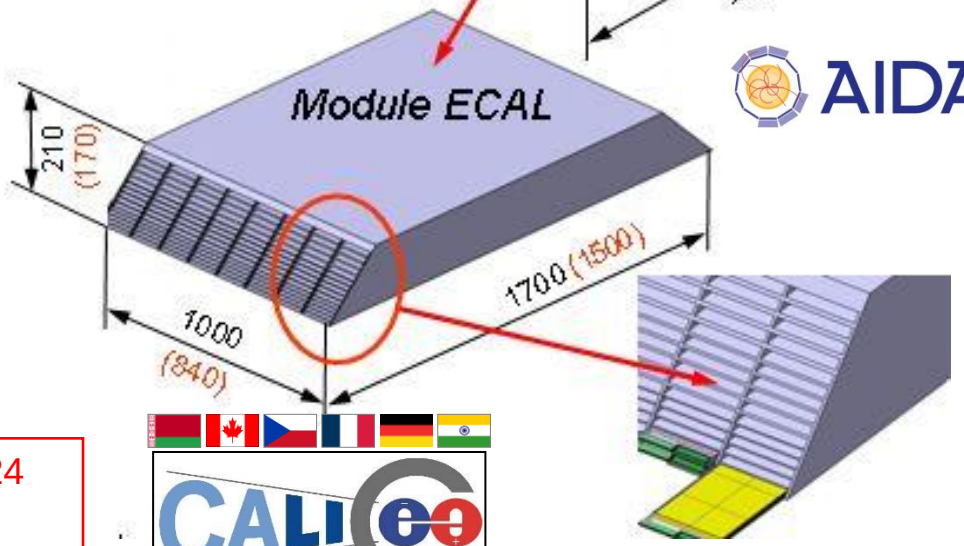


Technological prototype : ECAL module

- Front-end ASICs embedded in detector
  - Very high level of integration
  - Ultra-low power with pulsed mode
  - 0.35 µm SiGe technology
- All communications via edge
  - 4,000 ch/slab, minimal room, access, power
  - small data volume (~ few 100 kbyte/s/slab)
- « Stitchable motherboards »







Elementary motherboard 'stitchable' 24*24 cm ~500 ch. ~8 FE ASICS
1 FEV= 4 wafers 9X9 cm2 = 4x4 chips
skiroc2 64 ch => 1024 pads.