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SKIROC2, a Front-end Chip designed to readout the E-Cal of ILC

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SKIROC (Silikon pin Kalorimeter Integrated ReadOut Chip) is the very front end chip designed for the readout of the Silicon PIN diodes foreseen for the Electromagnetic CALorimeter (ECAL) of the future International Linear Collider.

The very fine granularity of the ILC calorimeters implies a huge number of electronics channels (82 millions) which is a new feature of "imaging" calorimetry.

Moreover, for compactness, the chips must be embedded inside the detector without any external component making crucial the reduction of the power consumption to 10 µWatt per channel. This is achieved using power pulsing, made possible by the ILC bunch pattern (1 ms of acquisition data for 199 ms of dead time).

Summary 500 words

SKIROC2 is a 64-channel front-end chip, designed in AMS 0.35µm SiGe technology.

The analog part has been designed to handle a dynamic range from 0.1 MIP (1Mip=4 fC) up to 2500 MIPs. The detector capacitance has been estimated to 20pF taking account the 25mm2 pin diode and the PCB.

Each of the 64 channels is made on an input charge preamplifier. A common gain can be set by changing the feedback capacitor Cf using the Slow Control parameters. Each preamplifier is followed by a slow channel for the charge measurement and by a fast channel for trigger generation.

The fast channel is made of a high gain variable CRRC shaper (tp tunable between 50 ns and 100 ns thanks to the Slow Control parameters) and is followed by a low offset discriminator to auto trig down to 0.1 MIP. The threshold of the 64 discriminators is supplied by a common 10-bit DAC and a 4-bit DAC per channel for each discriminator. Each discriminator output is sent to an 8-bit delay cell (delay time tunable between 100 ns and 300 ns using the Slow Control parameters) to provide the Hold signal for the slow channel. A wired OR of the 64 triggers is available (trig_outb).

The slow channel is made of a low gain and high gain CRRC shapers to handle the large dynamic range in order to provide a filtered charge measurement. Each one is followed by a Track and Hold. As soon as there is an HOLD signal, the charge is stored in a 15 depth SCA as well as the time of each event (time tagging is performed thanks to a 12-bit TDC ramp).

The time and charges stored in the SCA cells are then converted by a 12-bit Wilkinson ADC and sent to an integrated 4 Kbytes memory.
The power consumption has been optimized to reach an ultra low consumption: about 1.5 mW/channel. This chip can be power pulsed. Each stage can be individually shut down when not used.

Primary authors: Ms SEGUIN-MOREAU, Nathalie (OMEGA / IN2P3 - CNRS); Mr CALLIER, Stéphane (OMEGA / IN2P3 - CNRS)

Co-authors: Dr DE LA TAILLE, Christophe (IN2P3 / CNRS); Mr DULUCQ, Frédéric (OMEGA / IN2P3 - CNRS); Dr MARTIN-CHASSARD, Gisèle (OMEGA / IN2P3 - CNRS)

Presenter: Ms SEGUIN-MOREAU, Nathalie (OMEGA / IN2P3 - CNRS)

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