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The Nectar GHz Digitizer ASIC for the Cherenkov Telescope Array

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The future international high energy gamma ray observatory, the Cherenkov telescope Array (CTA), will consist in an array of 50-100 dishes of various sizes and various spacing, each equipped with a camera, made of few thousands fast photodetectors and its associated front-end electronics. The total number of electronics channels will be larger than 100,000 to be compared to the total of 6,000 channels of the 5-telecopes H.E.S.S. array. To optimize the overall CTA cost, a consequent effort is done to lower the cost of the electronics while keeping performances at less as good as the one demonstrated on the current experiments and simplifying its maintenance. This will be allowed by mass production, taking benefit of the use of standardized modules and massive integration of front-end functions in ASICs. In the framework of the NECTAR program, supported by the French ANR, a new detection module, housing the photodetectors, their high voltage power supplies and the associated front-end electronics has been studied. As in the H.ES.S. camera, the front-end electronics architecture is based on the very early digitization at rate higher than the GHz of the photodetector signals performed by a wide dynamic range analogue memory ASIC. A new digitizer chip, called NECTAR0, integrating a 2-channel, 1024-cell depth, high speed analogue memory together with a 12-bit, 20MS/s ADC followed by a 240Mbit/s digital serializer. Its targeted performances (11.6 bit dynamic range, 3.2 GS/s maximum frequency, power consumption) are equivalent or better than the one of the previous generation of chips used in H.E.S.S. 2. . The paper describes both the architecture of this new chip and reports its measured performances within a realistic environment.

Summary 500 words

I. INTRODUCTION

The Cherenkov light generated by the electromagnetic showers produced by the interactions of very-high-energy gamma rays in the atmosphere is a short signal of few ns duration and ˜1° extension, when observed from ground by IACTs. These light pulses are imaged by a camera, which is a mosaic of fast photomultipler tubes (PMTs), located at the focal plane of each telescope. The PMT signal is integrated over a window (typically 6-10ns) which must be long enough respectively to the signal duration and as short as possible to avoid integration of night-sky background (NSB) and electronics noise fluctuation.

. The electronics power consumption has to be low to avoid complex and heavy cooling system and the weight of the camera has to be minimized to decrease the cost of mechanical structure and to reduce the telescope positioning time. Finally, for CTA, the overall cost of a camera channel, including the photodetector and the high voltage power supplies must be less than that 300 Euros, this is the target for the NECTAr demonstartor

II. THE NECTAR MODULE

Most of the stringent requirements for the CTA electronics can be achieved using analogue memories. The fast analogue input pulses are sampled and recorded in these memories, used as circular buffers, at rate of few GS/s and read back and digitized on demand with lower frequency when a trigger occurs. The signal integration is performed digitally by FPGA. This kind of architecture permits to use low power, low cost ADCs (rather than high speed flash ones) and to decrease drastically the rate and then also the price and the power consumption of the following digital electronics. The overall design of the NECTAr module, that reads 7 PMTs, is driven by cost reduction and high reliability. All its electronics is concentrated on a single board build around the new NECTAr digitizer chip. It also houses the high voltage power supplies and a single low cost FPGA controlling the module, processing the data and transmitting them using an ETHERNET interface.

III. THE NECTAR0 CHIP

The NECTAr0 chip performs the sampling, memorization and digitization of only two differential channels, whereas it will be 4 in the final one. It integrates two analogue memories, similar to those of SAM, but with depth extended to 1024 cells to deal with longer trigger latency.

Their outputs is multiplexed towards a pipeline 12 bit ADC working at 20 MHz which output data are serialized on 3 LVDS output to reduce the number of interconnections with the FPGA.

The chip main performances are targeted to be similar to those of the SAM chip (typically more than 11 bit dynamic range at sampling frequencies up to 3 GS/s for an input bandwith larger than 300 MHz) .The final paper will describe with more detail the chip architecture and report complete test results of the chip including

test with photodetectors.

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