The Data Acquisition Card for the Large Pixel Detector at the European-XFEL

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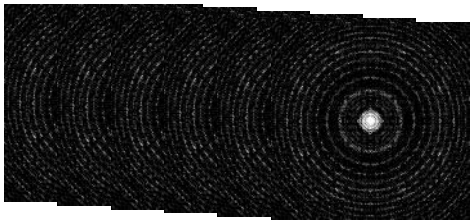
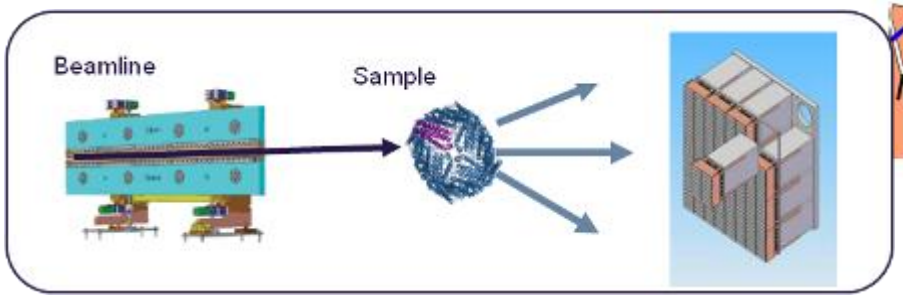
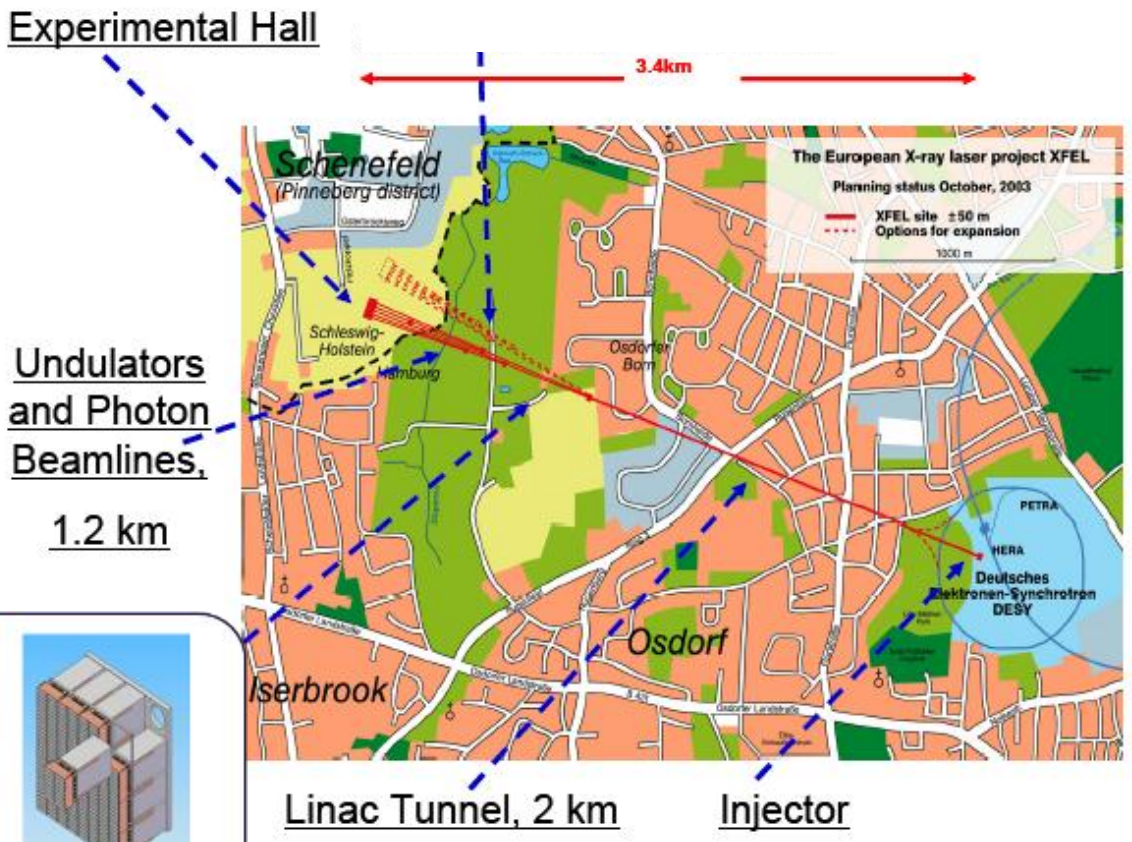
- European-XFEL
- Large Pixel Detector (LPD)
- LPD DAQ Card (FEM)
- FPGA Firmware 10G UDP/IP
- Status

European-XFEL DESY Hamburg



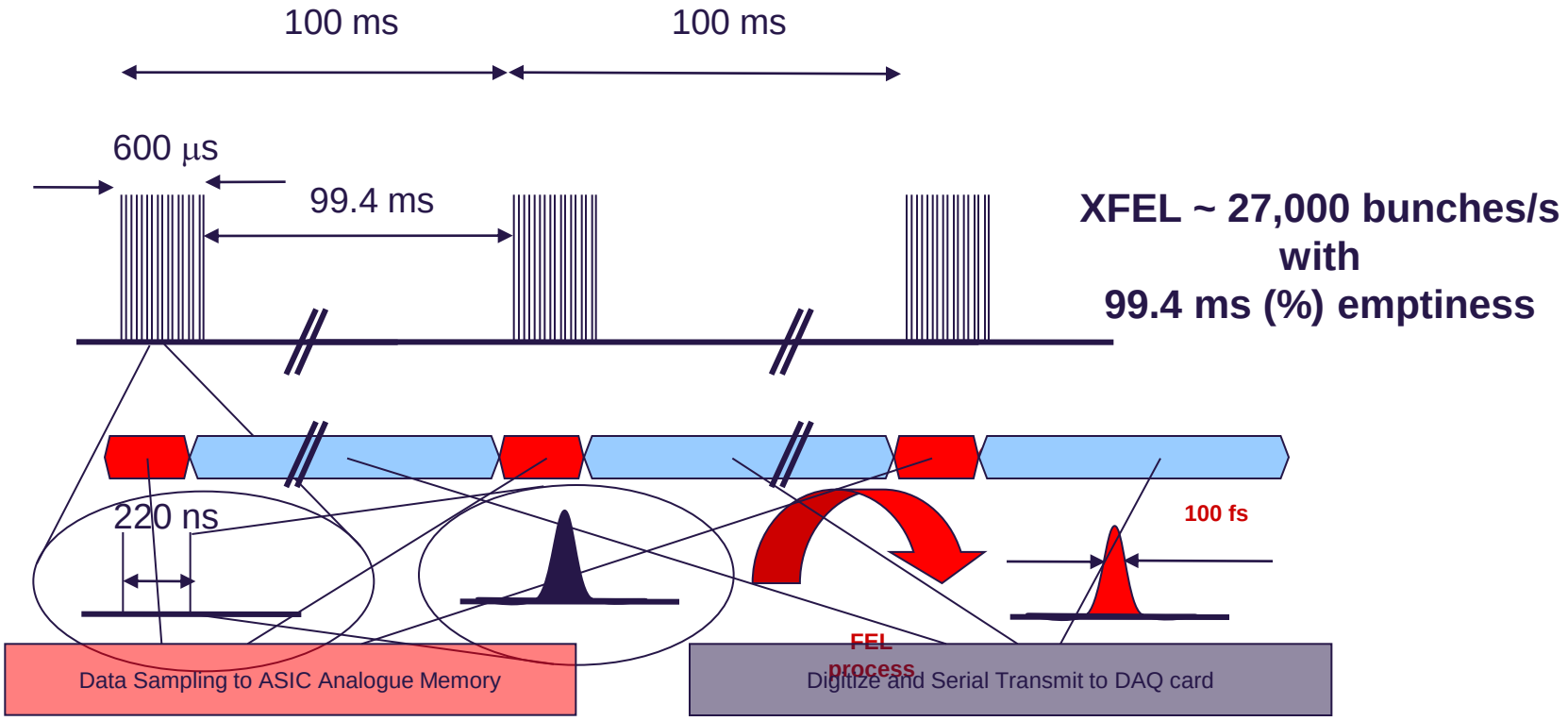




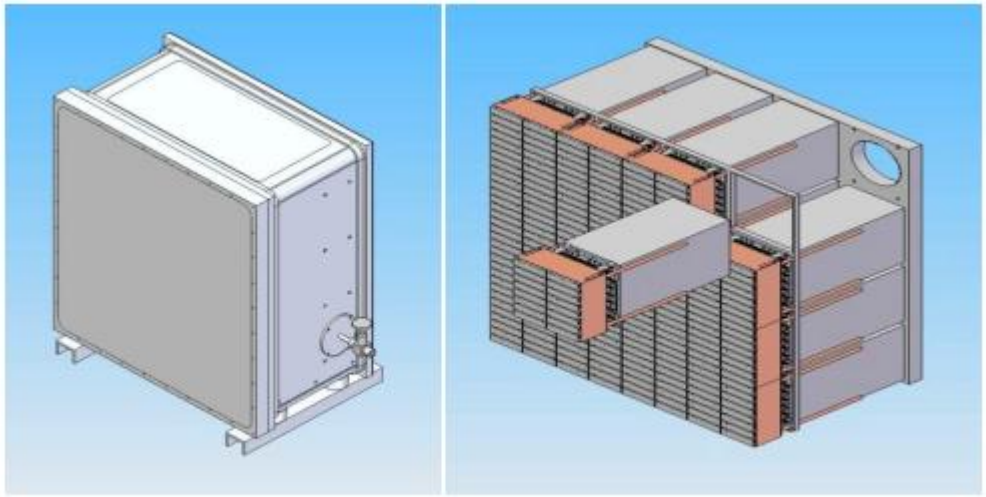
Experiments to start operation in 2015

Eu-XFEL Bunch Structure

Electron bunch trains; up to 2,700 bunches in 600 μsec, repeated 10 times per second.
Producing 100 fsec X-ray pulses (up to 27,000 bunches per second).



Large Pixel Detector



- 1 Mega-pixel Detector
- 0.5 m x 0.5 m
- 16 SuperModules (SM)
- 1 DAQ card per SM
- 128 ASICs per SM
- Delivery in 2013

Figure 1. 1Mega pixel prototype arrangement.

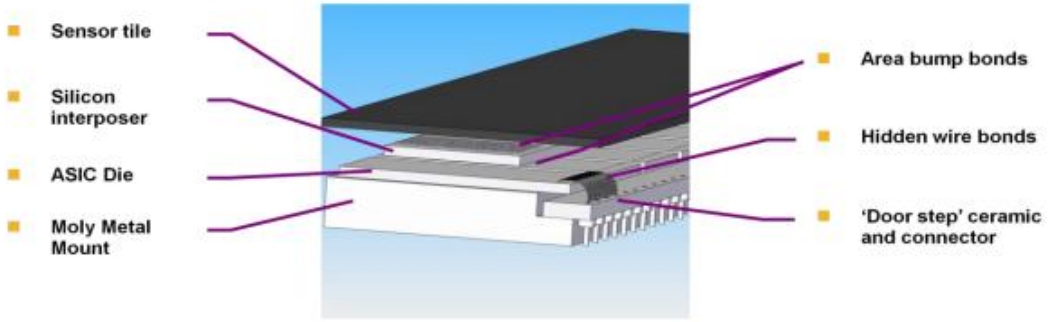
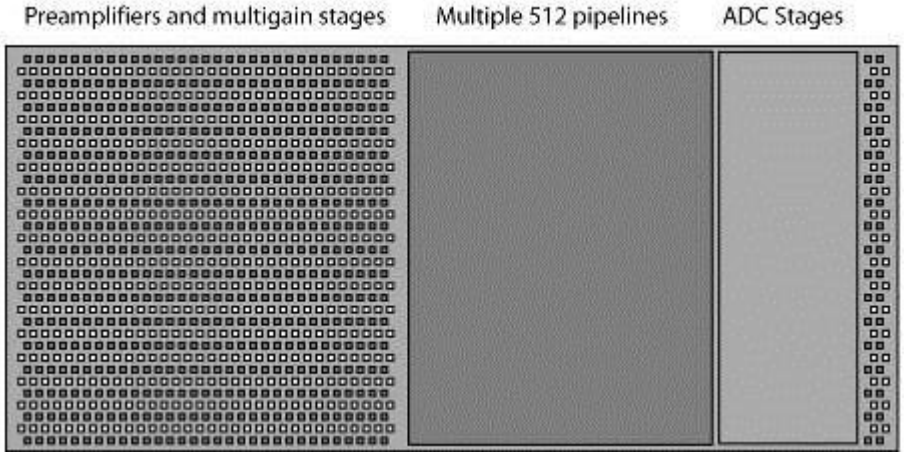
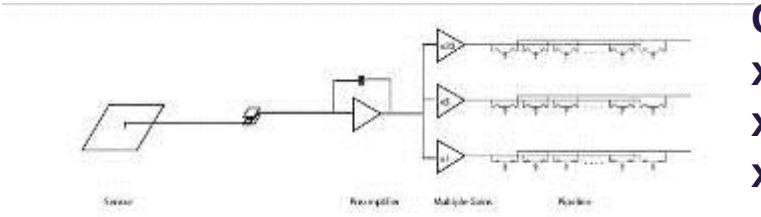


Figure 2. Module construction

- 16 sensor modules per SM

LPD ASIC





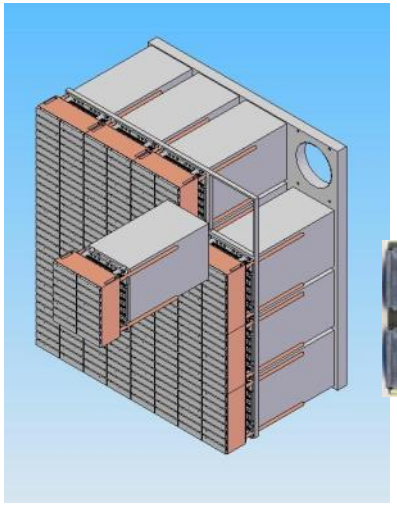
Gains
x 100
x 10
x 1

- 130 nm IBM
- 16 x 32 pixels
- Large Dynamic range
  ~1 – 10**5 photons
- 3 x Gains stored
- Analogue Pipeline Memory
- 512 samples deep
- Triggered Operation
- Digitise @12 bits and serial readout

Store in Pipeline during Bunch Train
Readout all 3 Gain values during long 99 msec gap

RAL Micro-Electronics
Paper submitted to IEEE NSS Valencia

LPD Data Acquisition

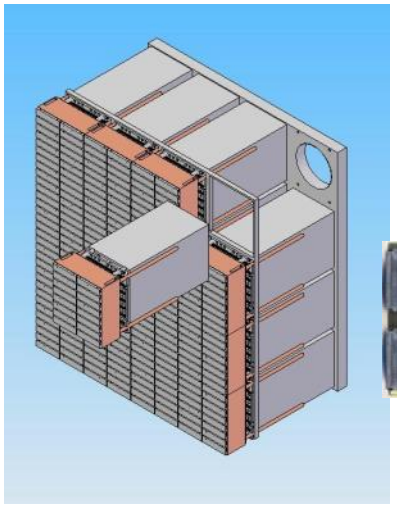


LPD Detector (STFC)

LPD DAQ Card FEM

x 16

XFEL Data Acquisition



LPD Detector (STFC)

LPD DAQ Card FEM

x 16

Fast Timing Signals

GbE Controls

MicroTCA (Physics Ext)

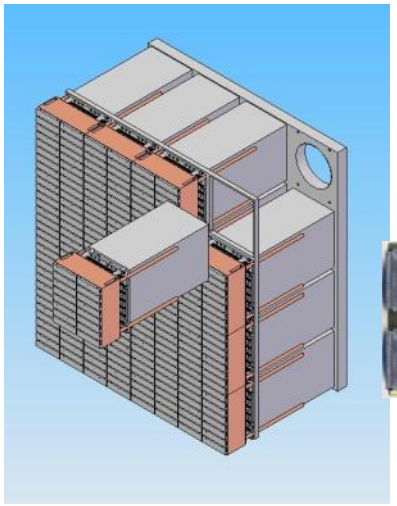
- XFEL Clock = 99 MHz
- Bunch Clock = 4.5 MHz
- Train Rate = 10 Hz

Clock & Controls and Veto Systems (UCL & DESY)

See Poster Session

XFEL Data Acquisition

- 2 MByte x 512 x 10
- ~10 GBytes/sec



LPD Detector (STFC)

LPD DAQ Card FEM

x 16

10 Gbps Optical
(DESY)

Fast
Timing
Signals

GbE
Controls

Train Builder System (STFC)
Data Readout
See Posters Session

AdvancedTCA

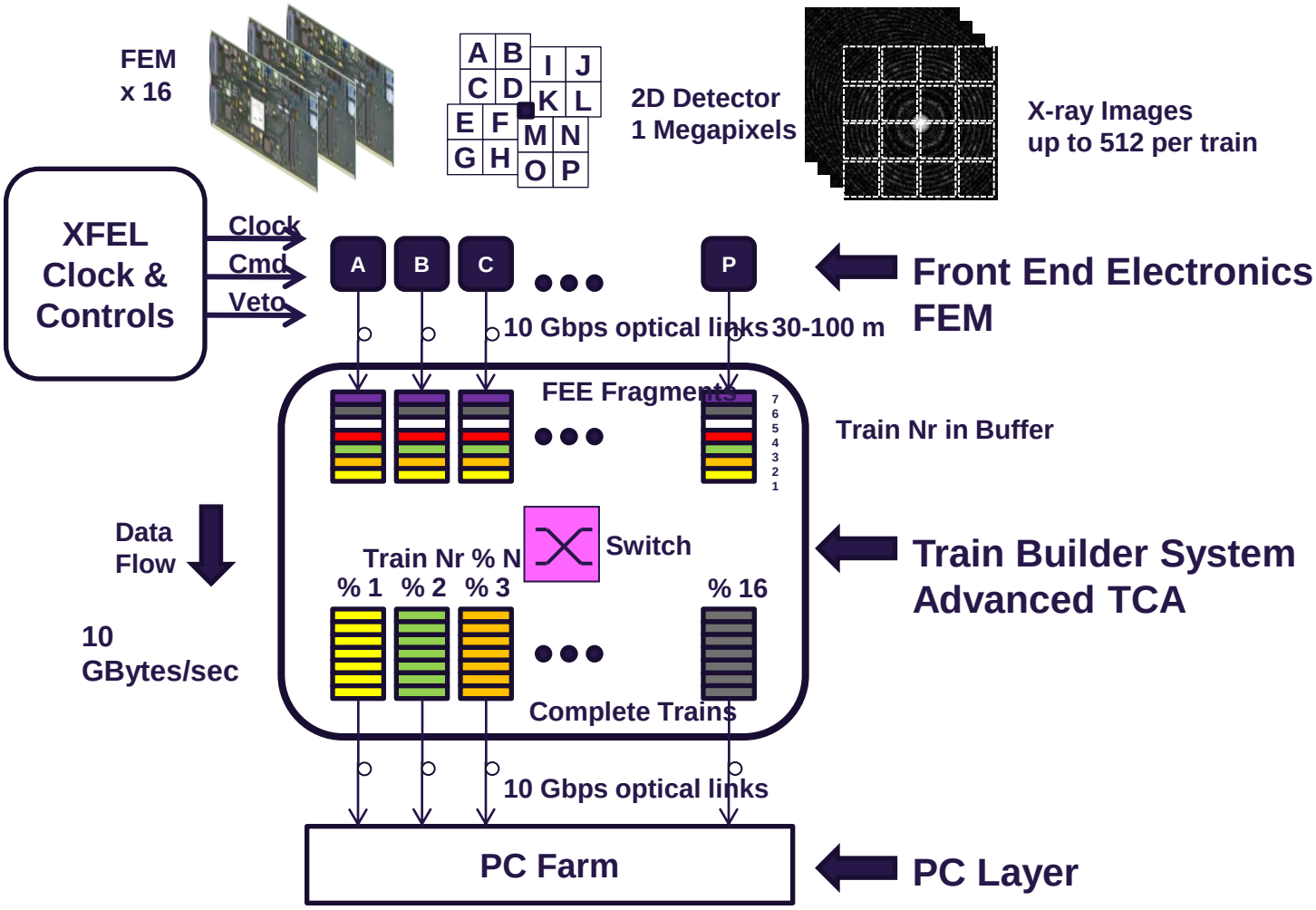
- XFEL Clock = 99 MHz
- Bunch Clock = 4.5 MHz
- Train Rate = 10 Hz

- Common Systems

MicroTCA (Physics Ext)

Clock & Controls and Veto Systems (UCL & DESY)
See Posters Session

Train Builder



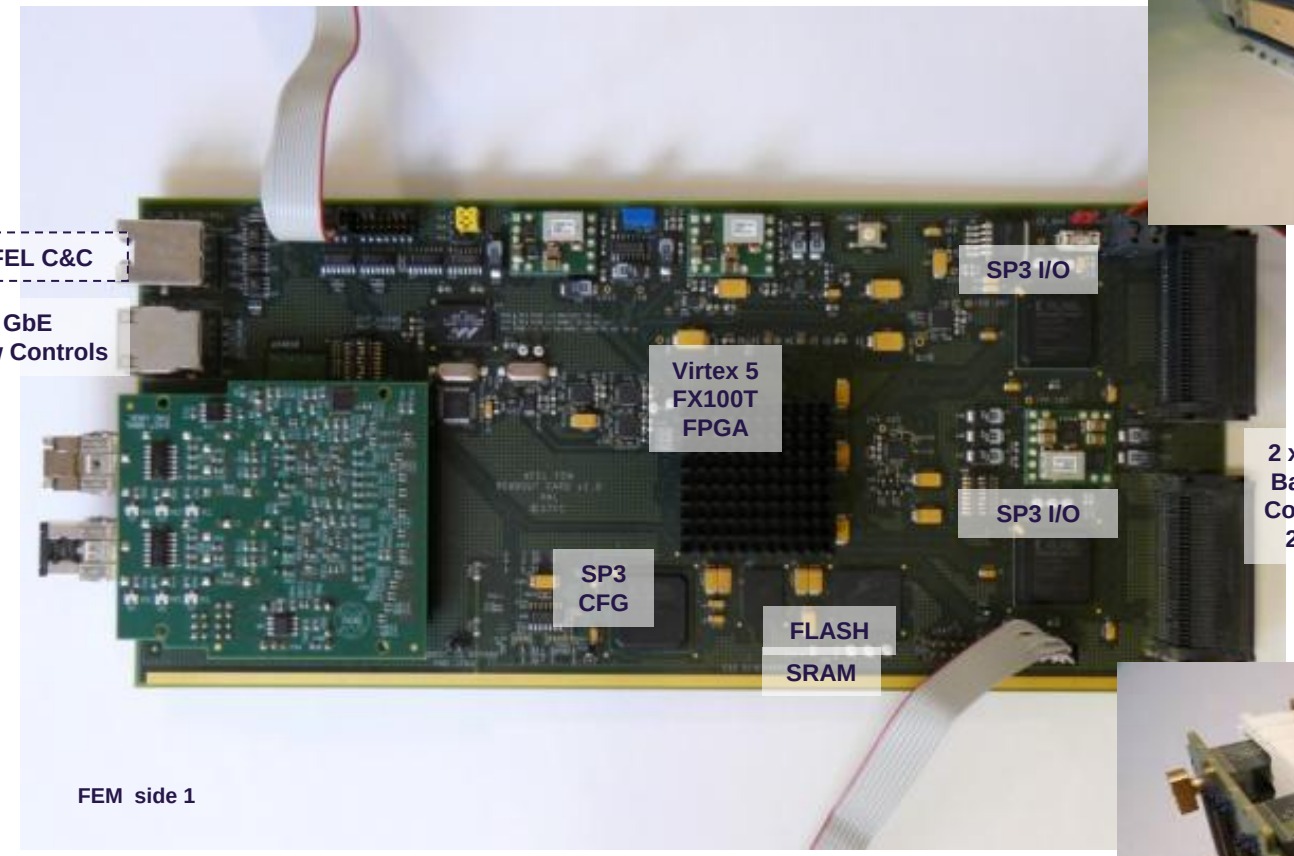
see Poster Session "Train Builder Data Acquisition System for the European-XFEL"

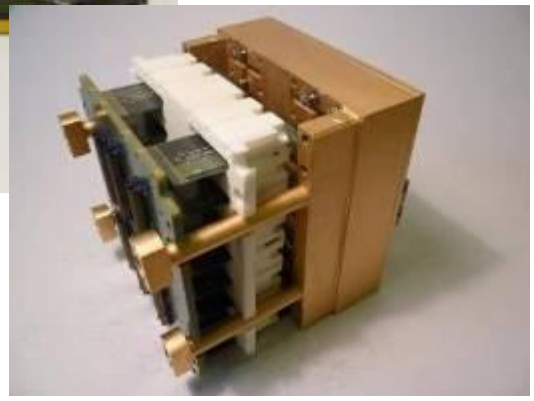
FEM Functional Units

- JTAG

FEM Clock Domains

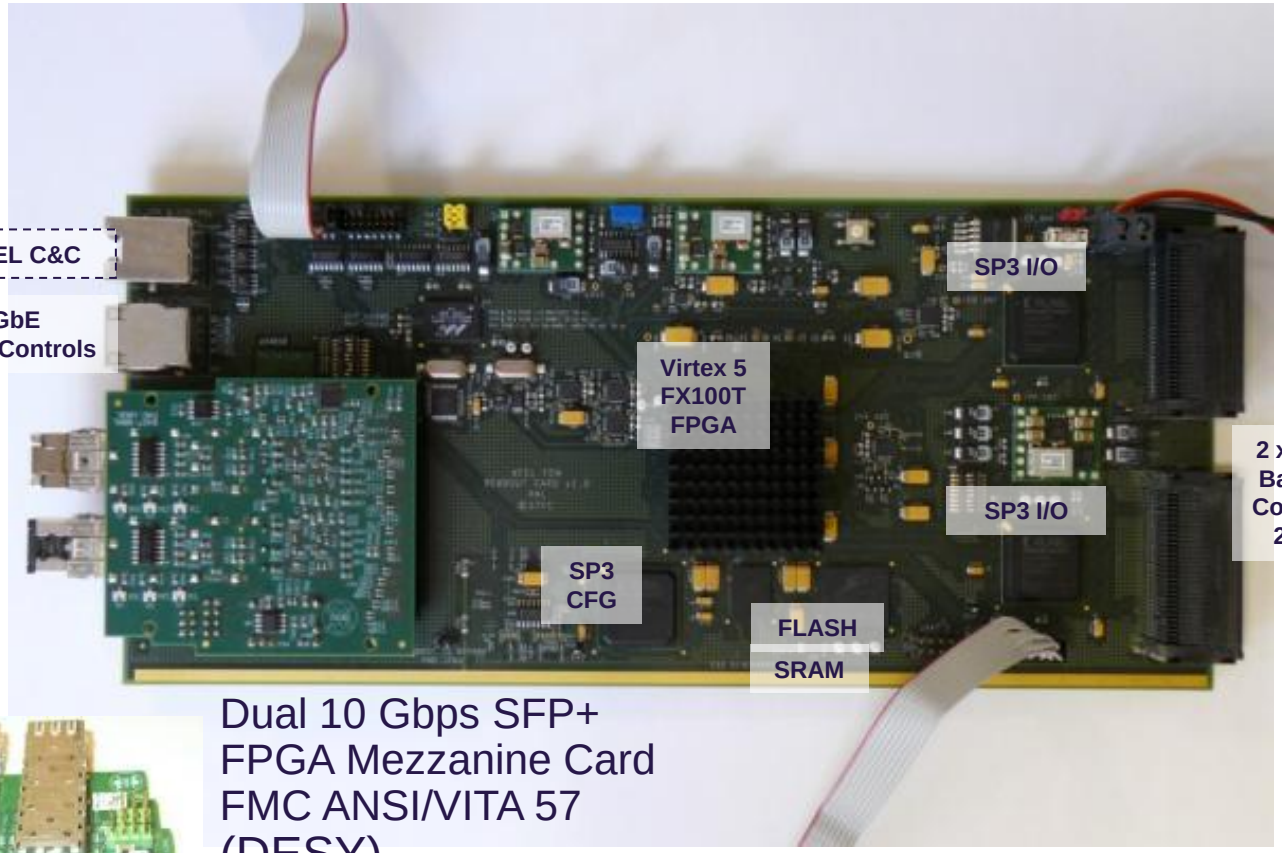
LPD FEM Side 1





128 LPD ASICs

LPD FEM Side 1



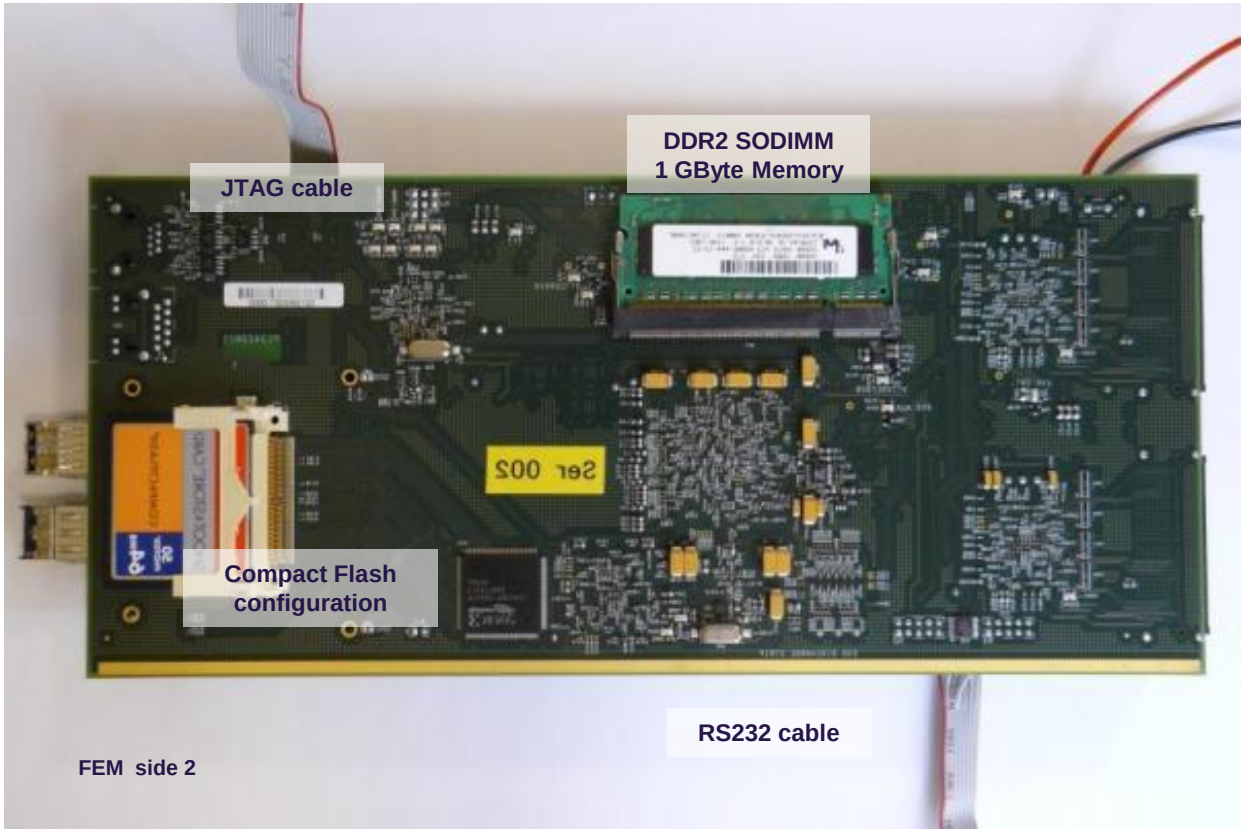
XFEL DAQ

LPD

Dual 10 Gbps SFP+
FPGA Mezzanine Card
FMC ANSI/VITA 57
(DESY)
Train Builder

LPD FEM Side 2

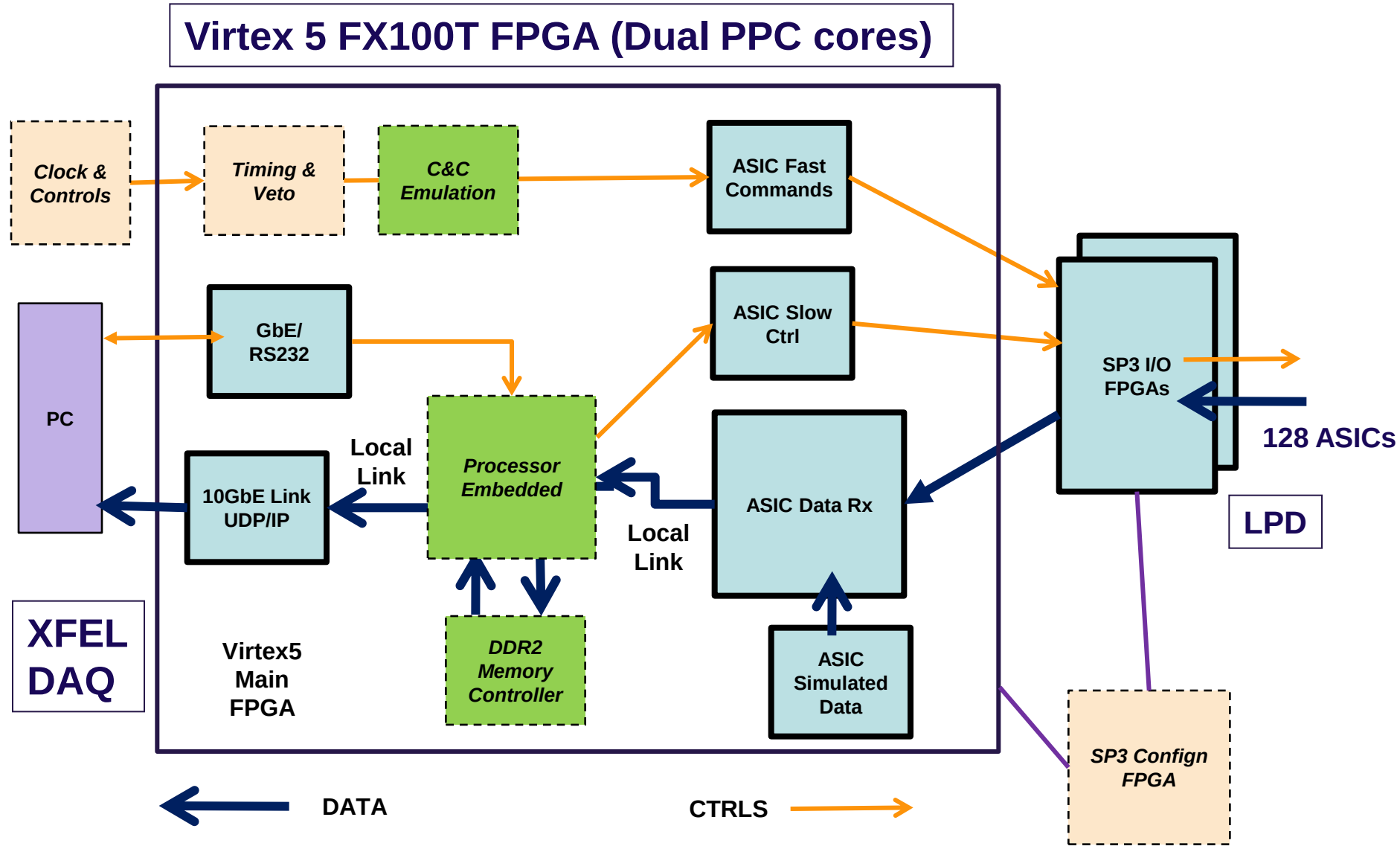
XFEL DAQ



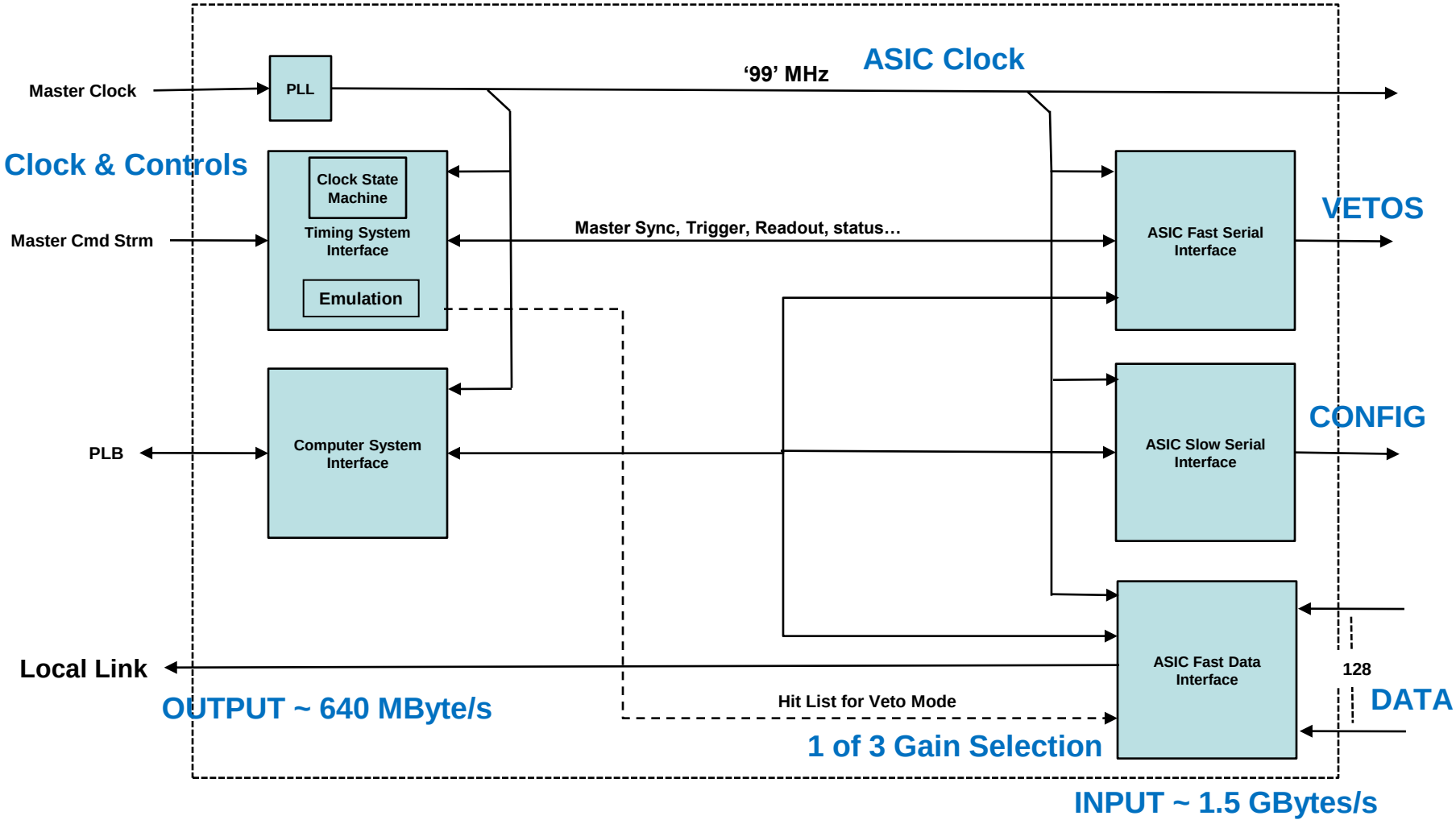
LPD

PCB 16 layers (8 signal)

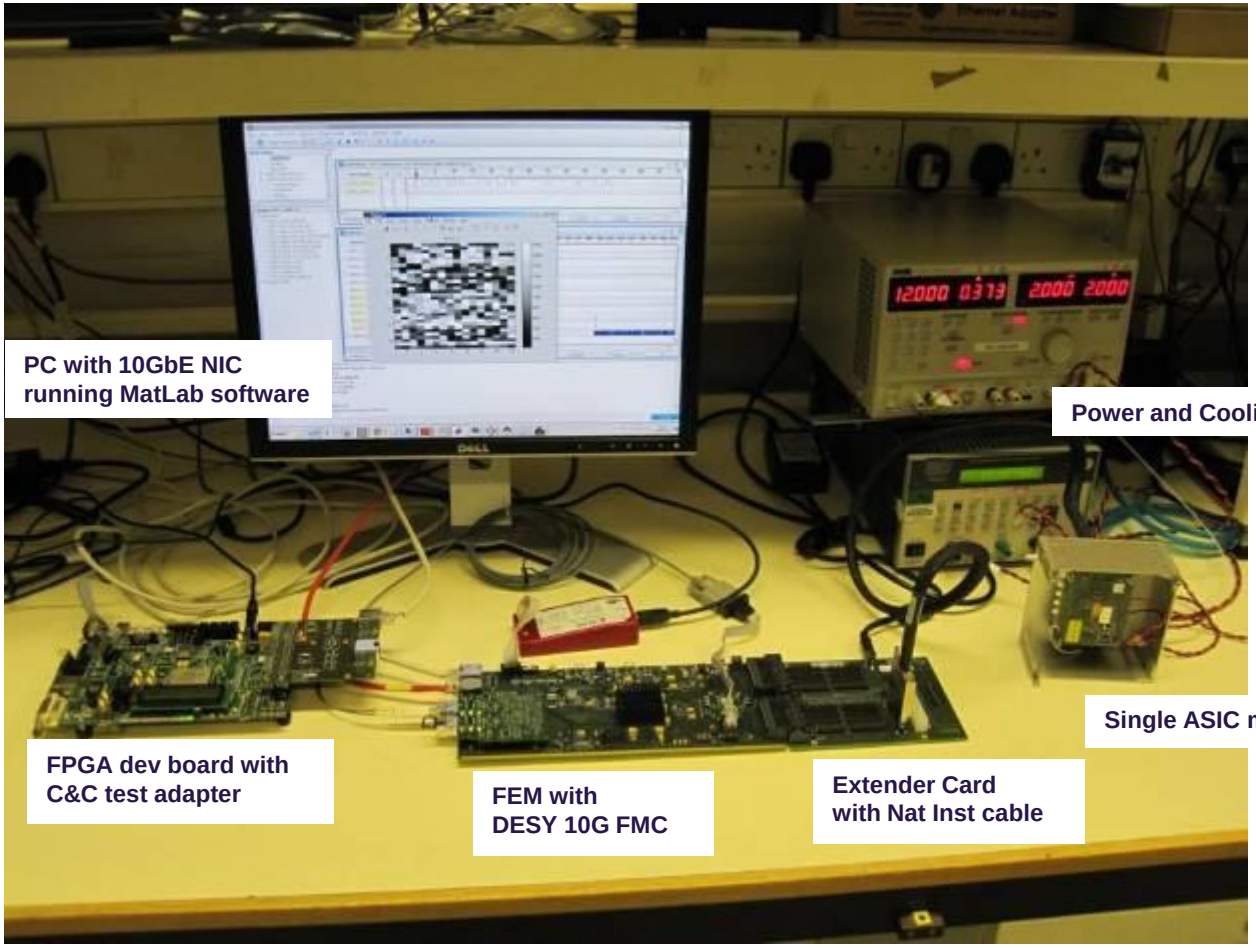
FPGA Units Overview

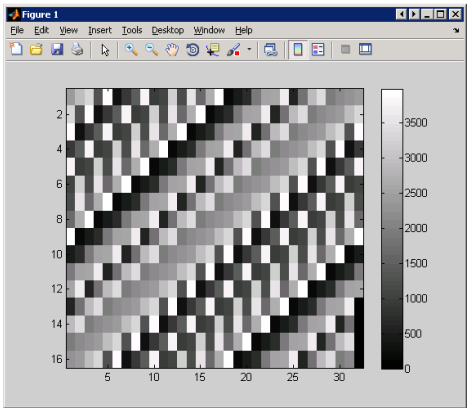


FPGA ASIC Unit



Testing Bench with LPD ASIC



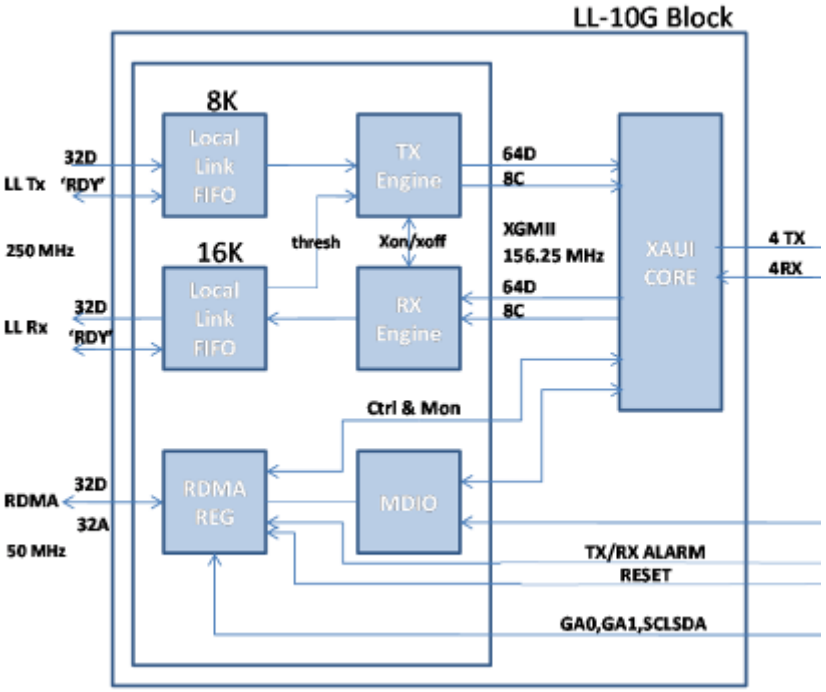


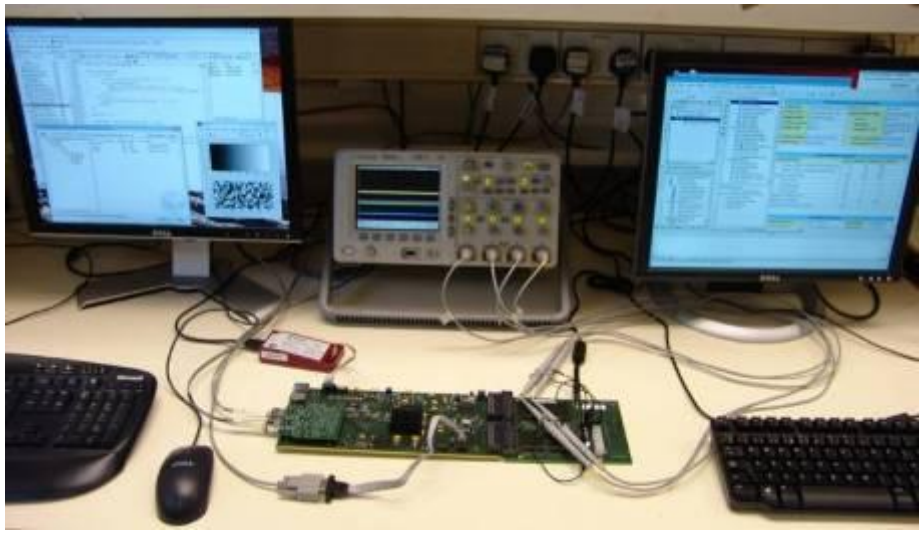
Pseudo-Random Data Image

- MatLab UDP
- RS232 control

FPGA 10G UDP/IP Firmware Module

Xilinx "Local Link" Interfaces to Power PC DDR2 Memory Controller And ASIC Data Receiver Module





10G Test Bench

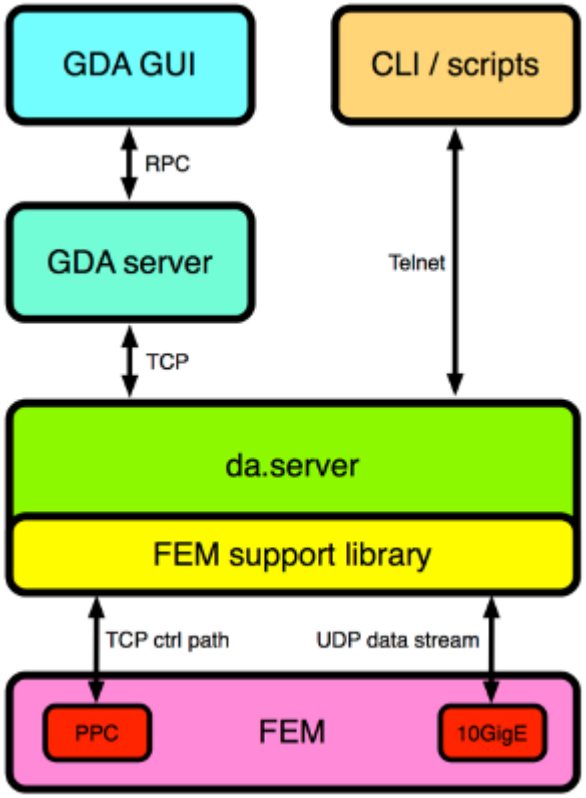
- Chelsio T4 NIC
  - Quad 10G SFP+
  - x8 PCIe Gen2
  - UDP API "Direct Driver" to App Memory

10GbE UDP/IP Firmware Module

LPD Software

- FPGA Embedded System Dual PPC Cores
- Core #1 for DDR2 DMA Memory Controller
- Core #2 Running Xilkernel / lightweight IP stack (LwIP)
- Have TCP control protocol over TCP/IP
- Control resources on board (GPIO, I2C, EEPROM)
- FEM support library library & applications (C & Python) for rapid prototyping developed
- GDA GUI based controls system as used on Diamond Light Source at Rutherford

PC Software



FPGA Embedded Software Xilinx EDK

FEM Status

- 4 FEM cards assembled. All passed JTAG without error.
- All components pass functional tests.
- FPGA 10G UDP/IP working with DESY FMC to PC NIC.
- Clock and Controls and Slow Controls GbE working.
- FEM reading out images from LPD ASIC module.
- Emulating Train Builder interface with FPGA dev boards.

- Manufacturing another 20 FEMs for LPD (and Medipix)
- Test FEM in LPD SuperModule in 2012
- Ready for LPD 1 Mega-pixel detector 2013

Thank you

Acknowledgements:
LPD Collaboration (STFC Rutherford Appleton Laboratory)
M. Zimmer, I. Sheviakov (DESY)
C. Youngman (XFEL)

Posters Session:

"Design of the Train Builder Data Acquisition System for the European-XFEL"
John Coughlan et al.

"Design and Development of Electronics for the EuXFEL Clock and Control System"
Erdem Motuk et al.