DC/DC ASIC CONVERTERS IN 0.35µm CMOS TECHNOLOGY

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Twepp 2011, Vienna 26-30 September 2011
Introduction

AMIS4

Design
  chip design & features
  bonding diagram
  protections

Tests
  efficiency results
  TID radiation test results

Conclusions
Power distribution with DC-DC converters

Constrains:
- magnetic (2T-4T) fields
- radiation (TID>100Mrd, fluence > $2\times10^{15}\text{ p/cm}^2$
  ions with LET<40MeV·cm²/mg)
## ASIC Design

<table>
<thead>
<tr>
<th>Feature</th>
<th>AMIS2</th>
<th>IHP1</th>
<th>IHP2</th>
<th>AMIS4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full control loop</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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</tr>
<tr>
<td>Dead times’ handling</td>
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<td>No</td>
<td>✓</td>
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</tr>
<tr>
<td>Soft Start</td>
<td>Simple RC</td>
<td>Simple RC with comparators</td>
<td>Full sequence with comparators</td>
<td>State machine</td>
</tr>
<tr>
<td>Over-I protection</td>
<td>No</td>
<td>No</td>
<td>✓</td>
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</tr>
<tr>
<td>Over-T protection</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>✓</td>
</tr>
<tr>
<td>Under-V disable</td>
<td>No</td>
<td>No</td>
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- **Used in system tests**
- **Taped-out Jan2011 still under tests, preliminary results**

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OUTLINE

- Introduction

- AMIS4
  - Design
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    - bonding diagram
    - protections

- Tests
  - efficiency results
  - TID radiation test results

- Conclusions
Some features integrated in the prototype:

- Bandgap
- 4 linear regulators: Pre-Reg, Analog, Digital and Driver
- Handling of the dead time with adaptive logic
- Triplication and logic against SEU and SET
- Improved power transistors’ design to reduce TID effects
- Possibility to enable only 2/5 of the power transistors for small Iout

Enablers
- Complete circuit
- Dimension of the power transistors

Protection
- Over-Current
- Over-Temperature
- Input Under Voltage

State machine for more reliable start-up procedure and handling of the signal from protection circuitry and Power Good signal generation

External components needed:
- Capacitor for one linear regulator
- Capacitor for Bootstrap
- Inductor
- Input and output capacitors
NEW LAYOUT AND BONDING

The pad disposition on-chip is very different than in our previous designs. This has been done to minimize the on-chip power distribution and optimize the number of bonding points.
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Vin

Low Side

High Side

Drivers

Ground

Phase

Vin

High Side

Phase

Low Side

Ground

L

I_L

C_out

Vout
New layout and bonding

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The ASIC will be packaged in QFN48 for first testing phase, then in QFN32 for system tests. This bonding diagram is feasible for mass production.

**QFN48, 7x7 mm²**

**QFN32, 5x5 mm²**
Power transistors have been carefully for maximum efficiency for
I_{out}=1-3\,A
L=200\,nH-400\,nH
f=1-3\,MHz

With an external pin only \( \frac{2}{5} \)th of the switches can be enabled
This allows having less power dissipated in switching and driving operations
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Linear regulators

Regulator

High Voltage (Reg_HV)

Analog (Reg_Control)

Digital (Reg_Control)

Driver (Reg_Driver)

Vin 10-12V

Vreg_HV 3.3V

1.2V

3.3V

3.3V

3.3V

Vdd_A

Vdd_D

Vdd_driver

Reg_HV, Reg_Controls are designed with fully integrated output capacitor

Reg_Driver requires 100nF external capacitor
Soft start allows a rise time of the Vout in around 10ms, avoiding too high in-rush current at the start-up.
Input Under – Voltage Protection

Vin

5V

4V

time (s)

converter off

converter on

converter off

Enable of the converter

Threshold
Over-Temperature Protection

Temperature

80°C

40°C

time (s)

Temperature

Enable of the converter

Threshold

converter on

converter off

converter on
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AMIS4

Chip available beginning of August
Still under test, preliminary results
Efficiency
AMIS4 QFN48(1/2)

Vin=10V, Vout=2.6V, L=460nH, f=1.35MHz, QFN48

Half switch enabled
Efficiency AMIS4 QFN48 (2/2)

Vin=8V, Vout=2.6V, L=460nH, f=1.35MHz, QFN48

[Graph showing efficiency versus output current with different magnetic inductances (L=460nH, T=+25°C, L=333nH, T=+25°C, L=220nH, T=+25°C, L=460nH, T=-30°C).]
Line and Load Regulation

\( V_{out} = 2.604V, \ L = 460nH \)

**Line regulation**

- 1.4MHz, 1.5A
- 1.4MHz, 3A
- 2.3MHz, 1.5A
- 2.3MHz, 3A

**Load regulation**

- 1.4MHz, \( V_{in} = 10V \)
- 1.4MHz, \( V_{in} = 8V \)
- 2.3MHz, \( V_{in} = 8V \)
Efficiency vs TID

L=397nH, f=1.35MHz, Vout=2.5V

\[\Delta \text{eff at } T=+25^\circ\text{C is 2.4\%} \quad (\text{max TID 96Mrad})\]
\[\Delta \text{eff at } T=-30^\circ\text{C is 31\%} \quad (\text{max TID 5Mrad})\]
**Efficiency vs TID**

$L=397\,\text{nH}, \, f=1.35\,\text{MHz}, \, V_{\text{out}}=2.5\,\text{V}$

Δeff at $T=+25^\circ\text{C}$ is 2.4%  
( max TID 96Mrad )

Δeff at $T=-30^\circ\text{C}$ is 31%  
( max TID 5Mrad )
Efficiency vs TID
Comparison AMIS2-AMIS4

Vin=10V, Vout=2.5A, Iout=1A

AMIS4, L=397nH, f=1.35MHz, T=-30°C,

AMIS4, L=460nH, f=1.35MHz, T=+25°C

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Efficiency vs TID comparison AMIS2-AMIS4

Vin=10V, Vout=2.5A, Iout=1A
Possible Issues

First tests have been done on a not optimized board (used for having easy access to all the pins)

In this board a large input voltage ripple has been detected.

A new compact board has been designed by Georges and in this days under tests

Preliminary tests show that the ripple is drastically reduced

Some issues sawn with large board need to be checked in the new board:

- noise in the VregHV (first regulator). It can be cleaned with an external capacitor
- inappropriate turn-off of the High-Side power transistor at f >2MHz with Vin>9V (this decrease the efficiency)
- over-current does not work (it can be disabled with a pin)
Efficiency AMIS4 QFN32

Plots I received few minutes ago from F. Faccio...
Future plans

Work to be done in AMIS4

A Focused Ion Beam will be used to modify some connection. This should solve some of the issues.

Irradiation test under Heavy ions and protons are foreseen in fall 2011

Definition of the bond-diagram for user applications (next weeks)

packaging (Europractice, ASE?) for system tests (fall 2011)

Work for AMIS5

Design of AMIS (fall 2011)

Submission (January 2012)
A new DC/DC converter ASIC called AMIS4 has been designed in a High Voltage 0.35um technology for automotive application. This technology has been successfully tested for TID, protons and heavy ions.

AMIS4 is a fully integrated synchronous buck converter which contains internal linear regulators, bandgaps, adaptive logic and a state machine to handle signals from the protection circuitry.

The converter is functional at for \( f \leq 2 \text{MHz} \) (only the Over-current is not working). Some issues have been detected at \( f > 2 \text{MHz} \) with \( V_{in} > 9 \text{V} \). A new test board has been designed and now under tests.

Efficiency is high (above 80%, also for high load 3-4A)

Radiation effects are limited (2-3% loss of efficiency over 100Mrad)

Line regulation is good (7 mV for \( V_{in} \) variation from 5 to 10V)

Load regulation is good (12 mV for \( I_{out} \) variation from 0 to 3.5A)
Vin=8V, Vout=2.6V, Iout=1.5A, T=+25°C