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DC/DC ASIC converters in 0.35um CMOS technology

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In view of the upgrade of the LHC experiments, we are developing custom DC/DC converters for a more efficient power distribution scheme.
Two new prototypes (AMIS3 and AMIS4) have been integrated in ASICs in the selected 0.35um commercial high voltage technology that has been successfully tested for all radiation effects: TID, displacement damage and Single Event Burnout.
While AMIS3 contains small incremental improvements with respect to previous prototypes, AMIS4 is a more complete converter that has been optimized for higher efficiency and improved radiation tolerance. Amongst the new features the most relevant are the presence of internal linear regulators, protection circuits with a state-machine and a new pinout for a modified assembly in package in order to reduce conductive losses.
The presentation will illustrate the design of the two prototypes, and show their functional and radiation tests.

Summary 500 words

In view of the upgrade of the LHC experiments, where the inner front-end electronics will require higher supply power, a new power distribution scheme has to be designed. A more efficient scheme, already presented at Twepp08, is based on custom designed step-down DC/DC converters able to work in the radiation and magnetic field environment of the LHC experiments (250 Mrad for TID, 2⊠1015 proton/cm2 for displacement damage ,4Tesla magnetic field). Specifications for the converter include an input voltage of 10-12V, output voltage of 1.2-3-3V, and output current of up to 3A.
A converter (AMIS2) has been already integrated in an Application Specific Integrated Circuit (ASIC) using a 0.35um commercial high voltage technology. This prototype, presented at Twepp09, has been successfully tested for radiations up to level required for experiment upgrades. Radiation effects covered both cumulative effects due to TID and displacement damage, and Single Event Effects –in particular Burnout.
Two new ASIC (AMIS3 and AMIS4) have been designed in the same semiconductor technology. AMIS3 is based on the same design used for AMIS2, but it includes a linear regulator and a different ramp generator. The first allows supplying the 3.3V needed by the control circuit and the drivers for the power switches directly from the 10-12V input voltage. The new ramp generator renders the converter capable to reach a 100% duty-cycle.
AMIS4 is instead a completely new design in this technology, based on experience obtained with 2 successive prototypes in a different 0.25um CMOS technology. It has been included in a Multi Project Wafer run in January and samples should be delivered to CERN in June. It contains four individual linear regulators to power at 3.3V different sections of the ASIC from the unique 10-12V input voltage. A first pre-regulator, with loose requirements on its output voltage, generates the 3.3V powering the bandgap reference circuit and the control circuitry of the other three regulators, each of them in turn regulating the supply to a separate domain: one for the drivers of the power transistors (very large current demanded for switching), one for the sensitive analog circuitry and one for the noisy digital circuits. The last two regulators and the pre-regulator have been designed to avoid the need for an external capacitor, decreasing the number of on-board components for the full DC/DC.
The chip has been engineered to obtain the highest efficiency compatible with the available semiconductor and assembly technologies. Choices on the power transistors'sizing and layout have been taken to that purpose for the range of specified output power conditions. The position of the bonding pads has been tailored to a bonding scheme on a QFN32 package reducing conductive losses. On a functional level, a sophisticated circuit handles the cyclic dead time (defined as the time when both power transistors are off to avoid cross conduction between Vin and ground)., granting a reduction of the switching losses in all the working modes of the converter - continuous and quasi-square wave.
Protections circuits as over-current, over-temperature and input under-voltage have been embedded in AMIS4. A state-machine handles the output of these circuits and allows a reliable start-up procedure.
AMIS2 tests for TID showed a drop of efficiency due to radiation-induced leakage current flowing along the edges of the power transistors. These have been redesigned in AMIS4 with a smaller number of edges to

reduce the TID effects. Furthermore radiation hardness has been improved identifying with simulations the circuit nodes sensible to Single Event Upsets and Transients (SEU and SET) and triplicating them to avoid error propagation to the control circuitry.
Other than the circuit design, functional and radiation test results of AMIS3 (delivery to CERN confirmed for the beginning of May) and AMIS4 will be presented at TWEPP.

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