# A radiation tolerant 5 Gb/s Laser Driver in 130 nm CMOS technology

Abstract : The GigaBit Transceiver (GBT) project aims at the design of a radiation tolerant chip set for high speed optical data transmission. The chipset includes the GigaBit Laser Driver (GBLD), a radiation tolerant ASIC designed in a standard CMOS 130 nm technology. The GBLD is a laser driver designed to work to up to 5 Gb/s and capable to drive both VCSELs and edge emitting lasers. The GBLD can provide modulation currents up to 24 mA and bias currents up to 43 mA. It also implements a pre-emphasis function to compensate for slow laser response or high capacitive load.

GBT project

The "GBT Project" is part of the "Radiation Hard Optical Link Project" which aims at developing a radiation hard bi-directional optical link for use in the LHC upgrade programs. The link targets data transmission between the on-detector and off-detector electronics serving simultaneously applications such as data acquisition, timing, trigger and experiment control. The GBT Project itself aims at the development of radiation hard chipset that will allow the implementation of such a link.
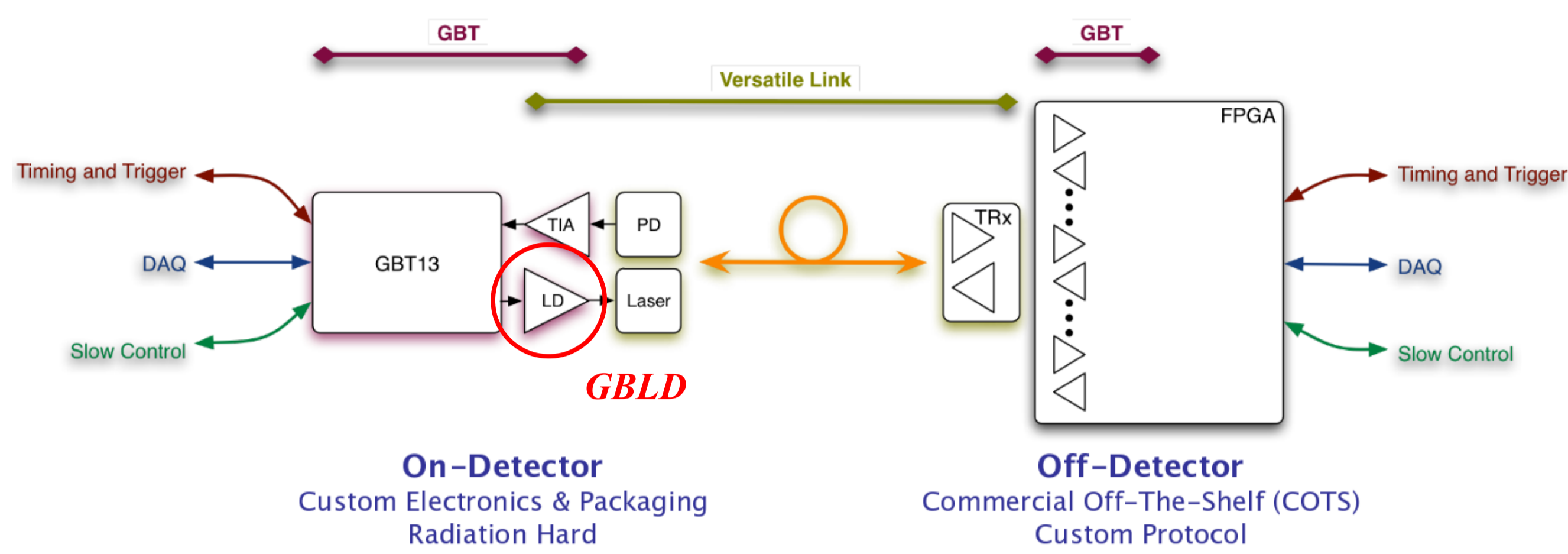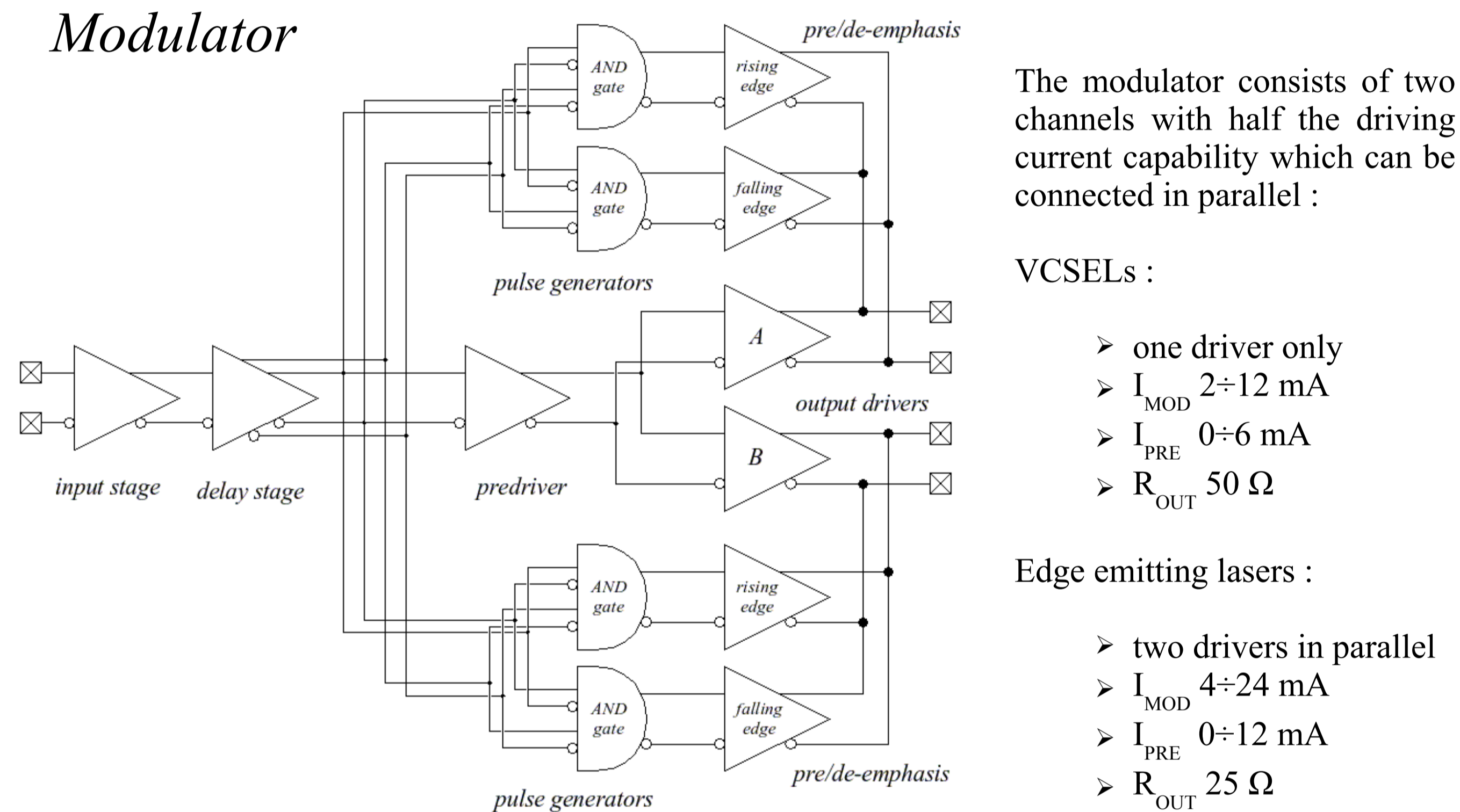

The GBt Laser Driver (GBLD)

The GBT chip set includes a laser driver (named GBLD) targeted at driving both VCSELs and some type of edge-emitting lasers at a maximum data rate of 5 Gb/s.
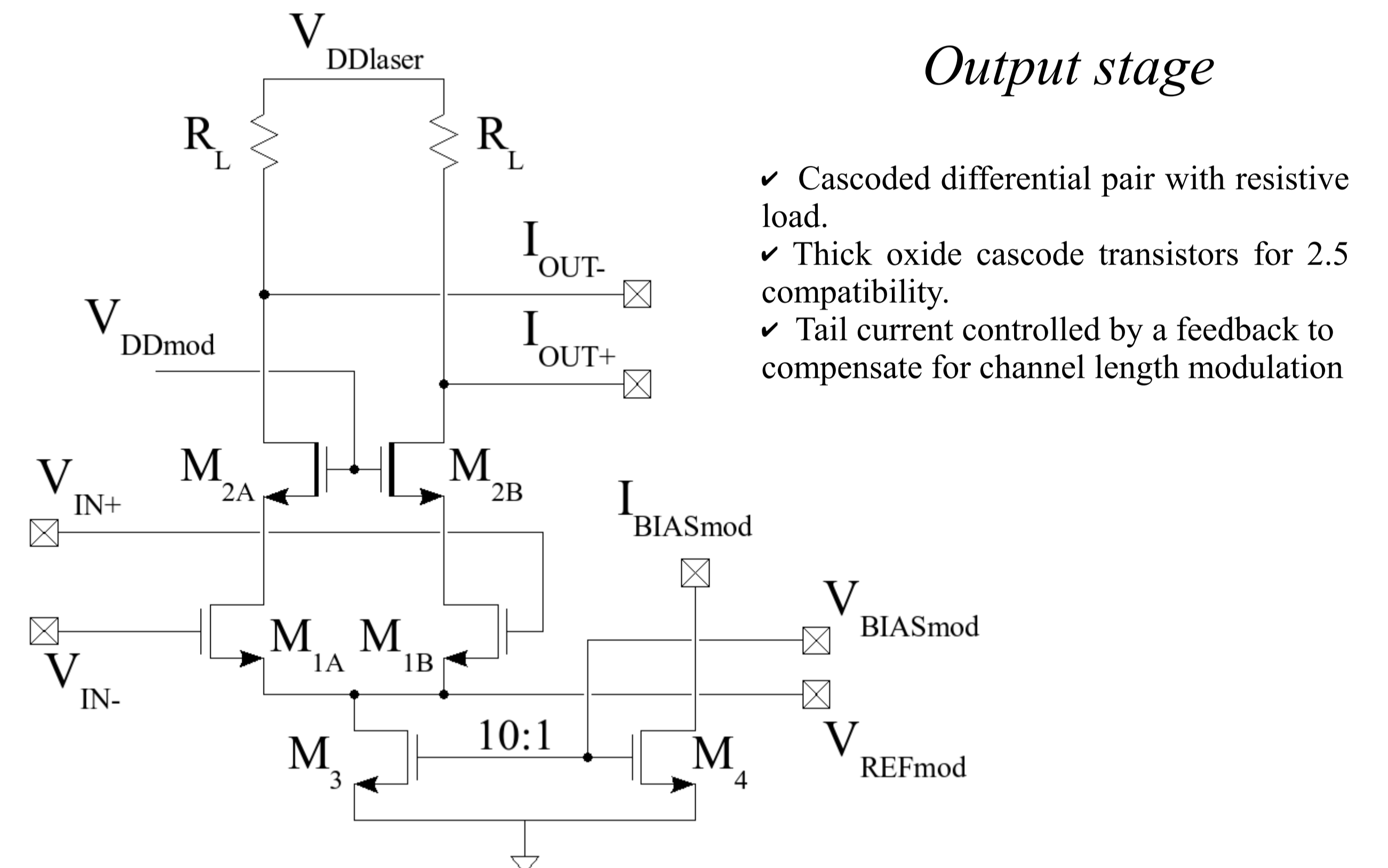
Main specifications :

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→ Bit rate	: 5 Gb/s
→ Modulation current	: 2-24 mA in 1.6 mA steps
→ Bias current	: 2-48 mA in 1.6 mA steps
→ Emphasis current	: 0-12 mA in 0.8 mA steps
→ Independently programmable pre/de emphasis	
→ Power supply	: single, 2.5 V
→ Random jitter	: < 1 ps (rms)
→ Deterministic jitter	: < 25 ps (rms)
→ Interface	: I^2C
→ TID protection	: deep submicron technology
→ SEU protection	: triple redundancy with self correction

Modulator

The modulator consists of two channels with half the driving current capability which can be connected in parallel :

VCSELs :

➢ one driver only
➢ I_{MOD} 2÷12 mA
➢ I_{PRE} 0÷6 mA
➢ R_{OUT} 50 Ω

Edge emitting lasers :

➢ two drivers in parallel
➢ I_{MOD} 4÷24 mA
➢ I_{PRE} 0÷12 mA
➢ R_{OUT} 25 Ω

Output stage

✔ Cascoded differential pair with resistive load.
✔ Thick oxide cascode transistors for 2.5 compatibility.
✔ Tail current controlled by a feedback to compensate for channel length modulation

Pre-emphasis

De-emphasis

Emphasis output driver

Measured eye diagrams

$I_{MOD} = 0$
$I_{PRE} = 0$

$I_{MOD} = 12.08$ mA
$I_{PRE} = 0$

$I_{MOD} = 7.12$ mA
$I_{PRE} = 3.6$ mA

$I_{MOD} = 12.08$ mA
$I_{PRE} = 3.2$ mA

Die photo / package
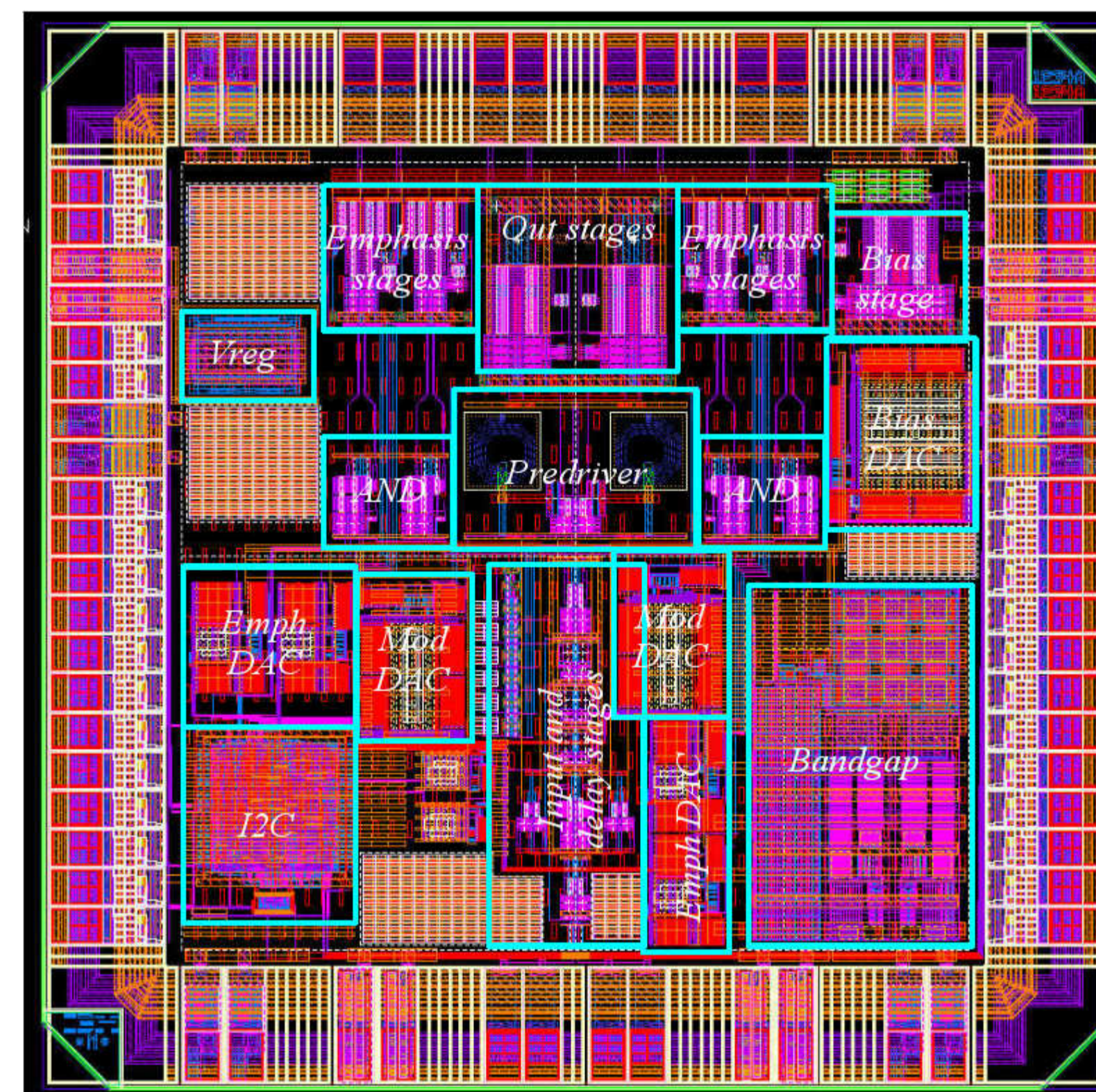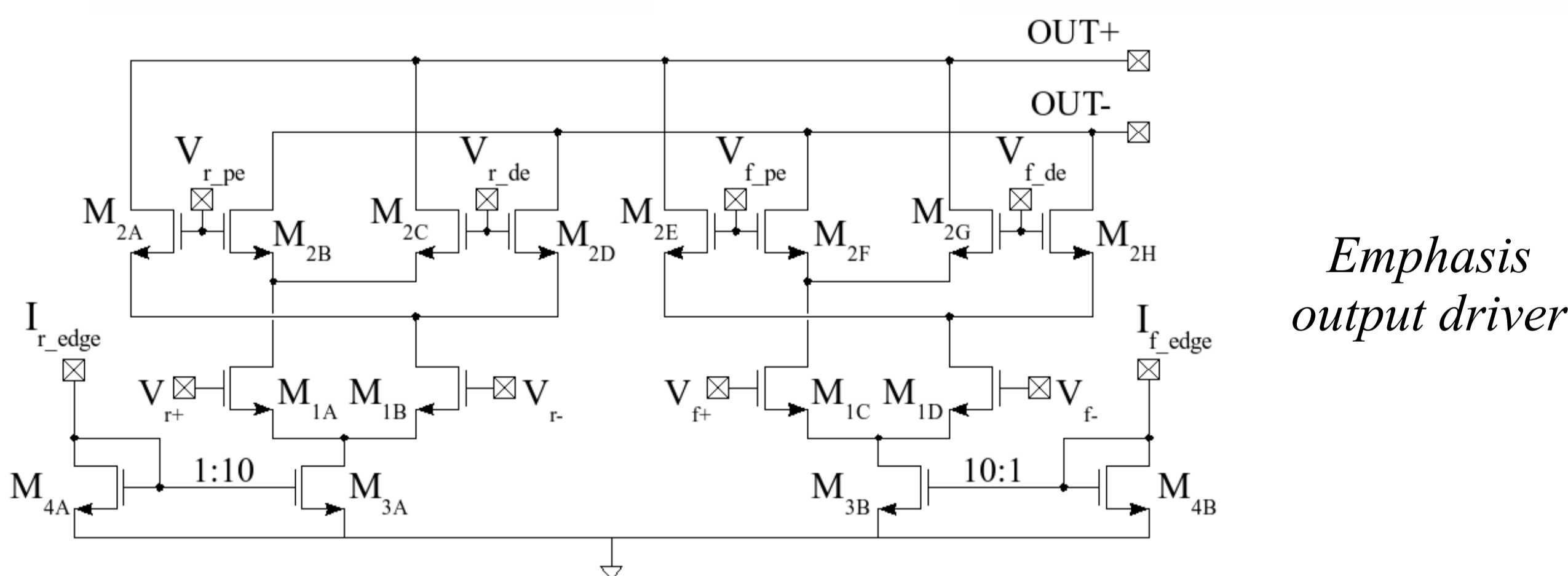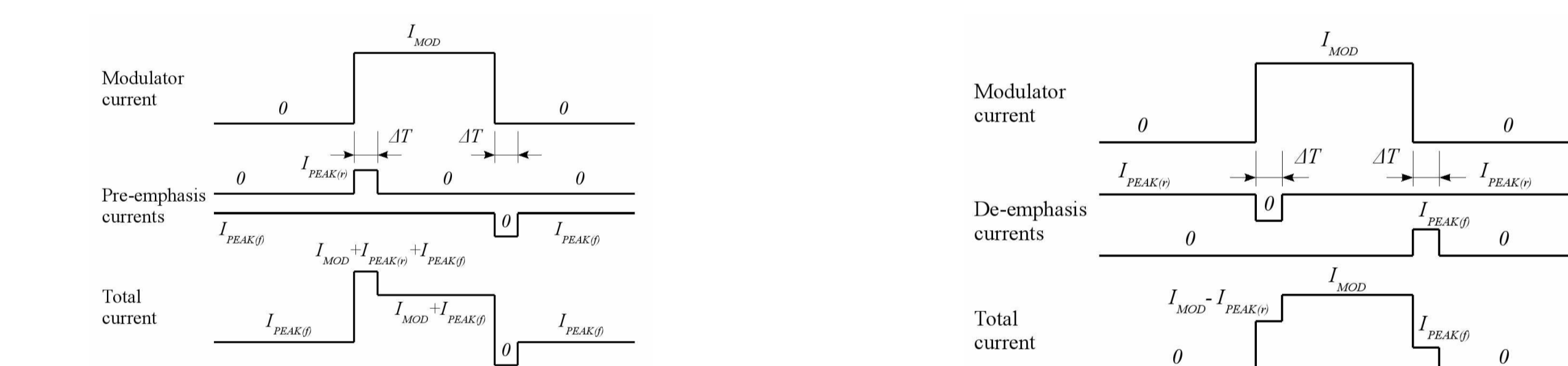
Technology	: CMOS 130 nm
Die size	: 2×2 mm²
Package type	: QFN 24
Package size	: 4×4 mm²
Configuration	: I^2C interface
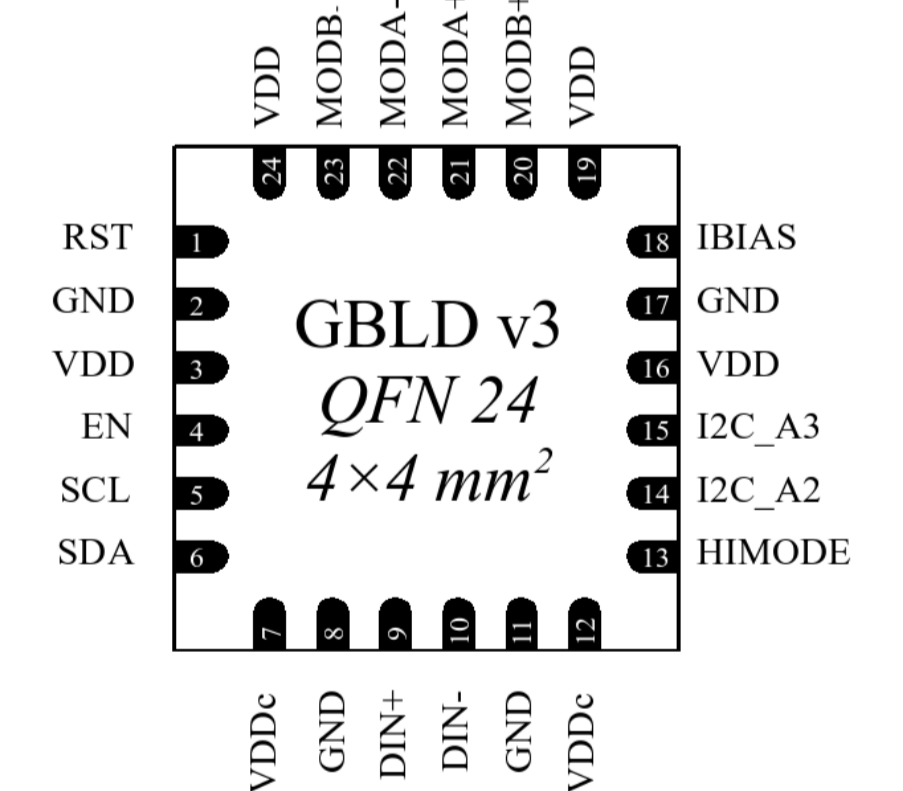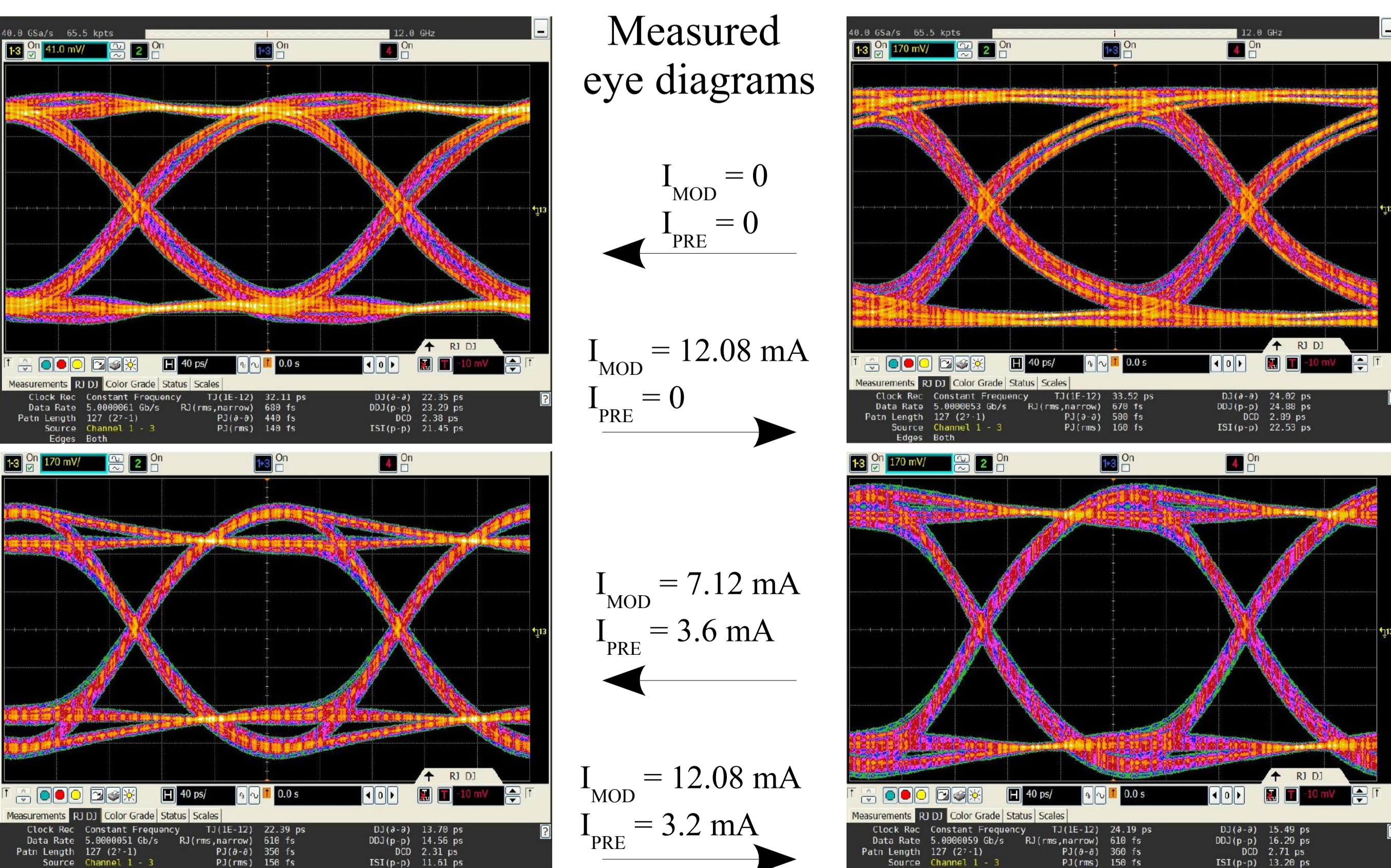
Jitter measurements

Tj   Rj   DDj
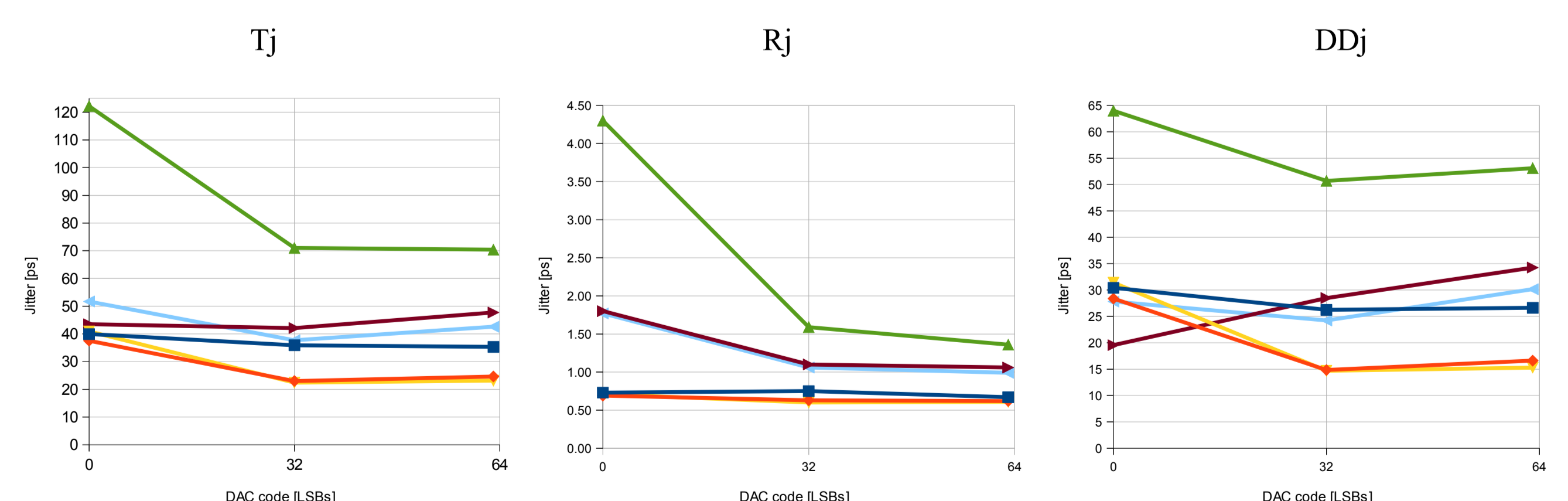
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