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A radiation tolerant 5 Gb/s Laser Driver in 130 nm CMOS technology.

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The GigaBit Transceiver (GBT) project aims at the design of a radiation tolerant chip set for high speed optical data transmission. The chipset includes the GigaBit Laser Driver (GBLD), a radiation tolerant ASIC designed in a standard CMOS 130 nm technology. The GBLD is a laser driver designed to work to up to 5 Gb/s and capable to drive both VCSELs and some types of edge emitting lasers. The GBLD can provide a modulation current up to 24 mA and a bias current up to 43 mA with the pre-emphasis function to compensate for external capacitive load.

Summary 500 words

The GBLD is a laser driver designed to target High Energy Physics (HEP) applications, where radiation effects are of major concern. It is part of a broader effort to design a radiation tolerant optical transceiver (the GBT project) for the future upgrades of the LHC experiments.

The GBLD is designed for a data rate up to 5 Gb/s and to drive both VCSELs and some type of edge emitting lasers. Its output stage is splitted in two halves, capable to drive a modulation current between 2 and 12 mA each with an output impedance of 50 ohm.

The two drivers can be connected in parallel in order to double the modulation current and to half the output impedance (for edge emitting laser application). The modulation current can be controlled via a 6 bit DAC with a resolution of 0.16 mA (when only one driver is connected) or 0.32 mA (when both drivers are connected in parallel). The GBLD also provides the laser bias current in the range 2 to 43 mA via an 8 bit DAC with a 0.16 mA resolution.

Pre- and de-emphasis can be applied independently on the rising and falling edge of the modulation signal, in order to cope with an asymmetric laser response. The emphasis pulse can be adjusted both in amplitude (between 0 and 12 mA) and in time (between 60 and 90 ps) by a 4 and a 2 bits DAC, respectively.

The driver is basically a cascade of resistively loaded differential pairs. The pre-driver stage, which is the most heavily loaded, make use of inductive peaking in order to increase the bandwidth.

The control DACs can be programmed via a I2C digital interface. Seven 8-bits control registers are used to store the configuration parameters. The control logic has been designed in order to be resistant to Single Event Upsets (SEUs) via Triple Modular Redundancy (TMR). An asynchronous correction logic has been adopted in order to provide error correction when the I2C clock is not present.

The chip is powered by a single 2.5V power supply, in order to use a single supply for both the laser diode and the laser driver. An internal voltage regulator brings down the voltage to 1.5 V for the internal circuitry.

A first version of the GBLD has been designed in a commercial 130 nm CMOS technology and packaged in a 4x4 mmˆ2 QFN24 plastic package.

The chip has been extensively tested in both the packaged and unpackaged versions, showing a random jitter between 0.6 and 1.8 ps and a deterministic jitter between 14 and 32 ps, depending on the modulation and emphasis settings. Such results have been obtained after a Focused Ion Beam (FIB) operation to reduce an over sized input protection diode.

The chip has been irradiated with X-ray up to 100 Mrad(SiO2).

This work describes in detail the operation principles of the GBLD circuits and the experimental results.

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