An FPGA based demonstrator for a topological processor in the future ATLAS L1-Calo trigger („GOLD“)

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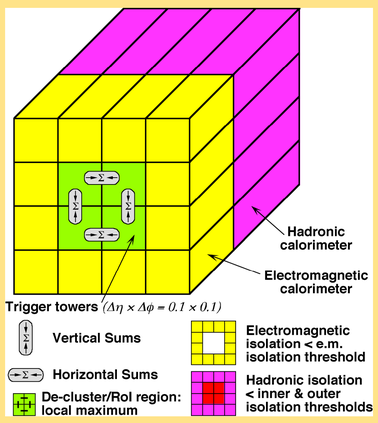
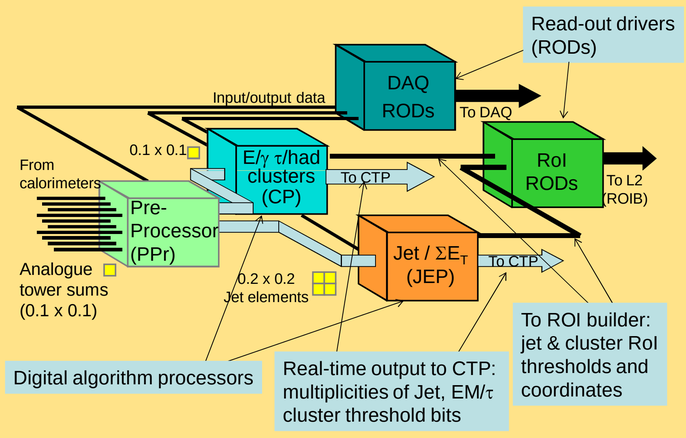
ATLAS Level-1 Calorimeter Trigger (L1Calo)

- Analogue data input from 7200 trigger towers($\Delta\eta x\Delta\phi$ = 0.1x0.1)
- Pre-Processor digitizes signals & makes bunch-crossing-identification (BCID)
- Digital signals fanned out to Cluster- (CP) & Jet/Energy-sum Processor (JEP)
- CP identifies electrons/photons and taus/hadrons
- JEP identifies jets & produces global sums of total, missing, and jet-sum energy
- Multiplicities of objects are sent to Common Merger Modules (CMM)
- CMMs produce results over crates & send them to Central Trigger Processor(CTP)
- Regions of Interest (RoI) are sent to LVL2 and Data Acquisition (DAQ) through Read-out drivers (ROD)

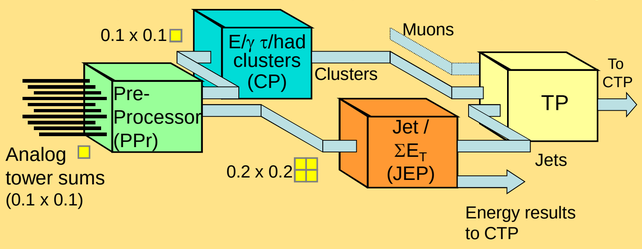




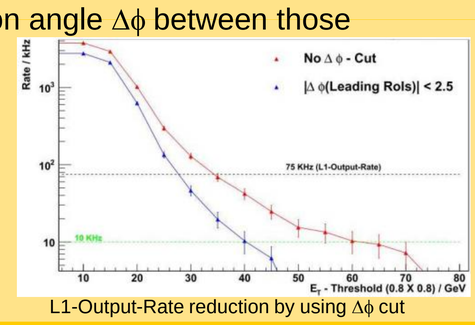
Existing L1Calo Components

LHC & L1Calo Upgrade

- LHC plans upgrade in 3 steps to increase the luminosity:
  - Phase 0 (2013/2014): L~1·10^{34} cm^{-2}s^{-1}
  - Phase 1 (2018): L ~ 2.5·10^{34} cm^{-2}s^{-1}
  - Phase 2 (2022/2023): L ~5·10^{34} cm^{-2}s^{-1}
- Currently Level1 is triggering on thresholds for global energy sums and count of objects(jets, electron, photon and tau candidates)
- Need additional trigger criteria for physics processes of interest to handle the increased event rate without raising thresholds : Topology!
- Need Topological Processor(TP) which should:
  - receive η, ϕ and transverse momentum(p_t) information of objects
  - run specific algorithms and send results to CTP
  - provide input bandwidth: e.g. JEP (~150 Gb/s) and CP (~450 Gb/s)
- High-luminosity Monte Carlo used to develop those algorithms
- Examples: sort out two jets with highest p_t and cut on angle $\Delta\phi$ between those



Part of L1Calo with new Topological Processor(TP)



L1-Output-Rate reduction by using $\Delta\phi$ cut

Generic Opto Link Demonstrator

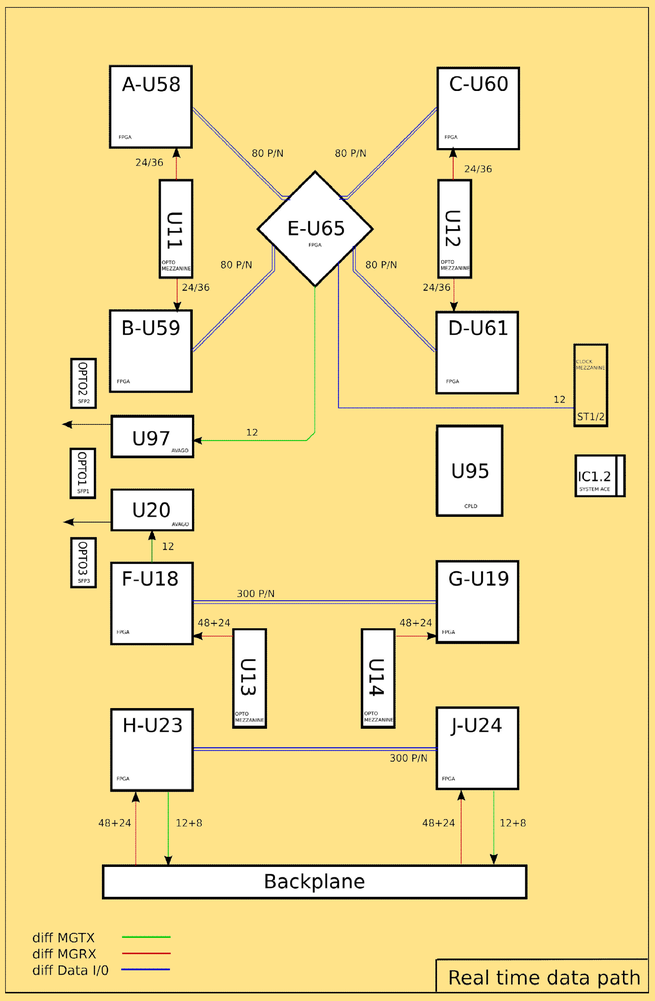
will explore the technologies needed to design the L1 Topological Processor.

Processing power is provided by

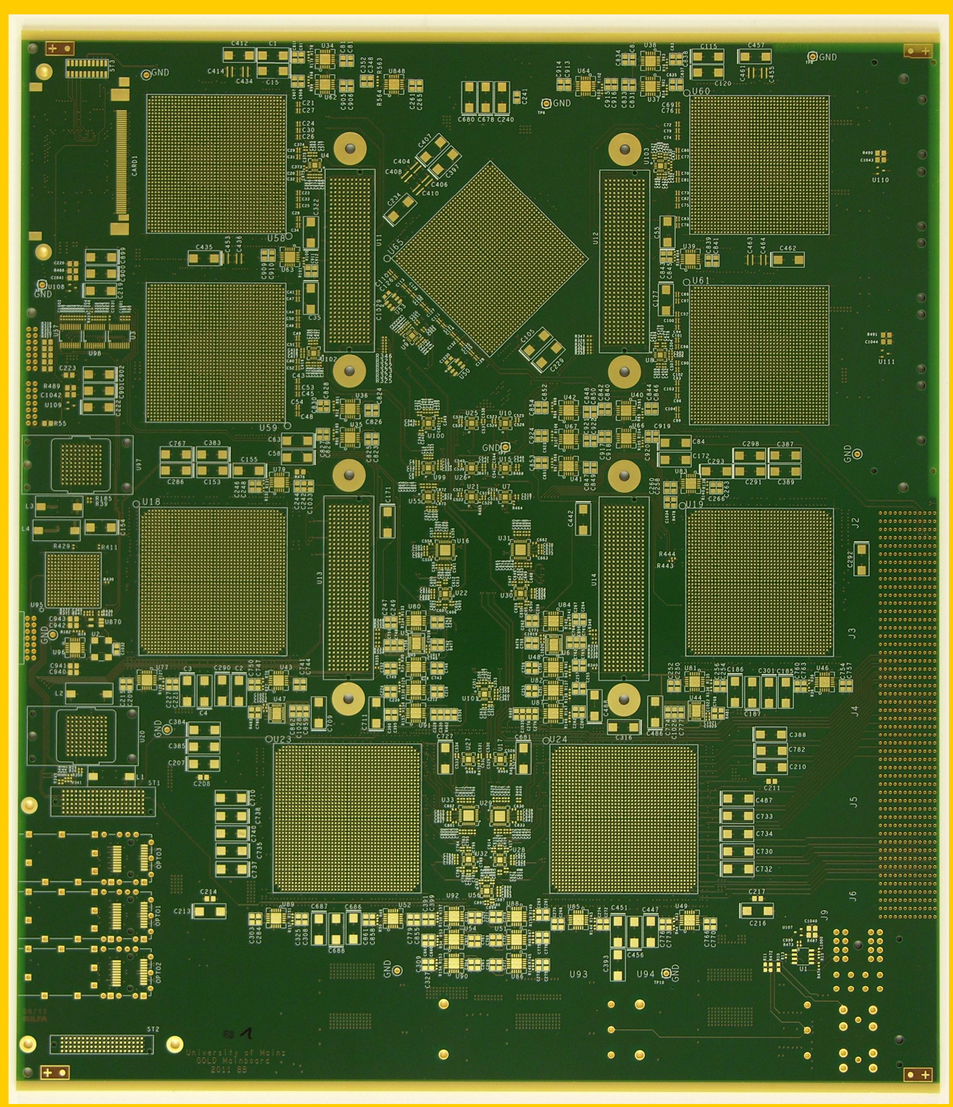
- Five **Virtex6-LXT240T(550T)** with 24(36) 6.4Gb/s MGTs
- Four **Virtex6-HXT380T(565T)** with 40 6.4Gb/s and 24 10Gb/s links

GOLD use cases:

- Demonstrator for AdvancedTCA module concept
- Demonstrator for Virtex-6 technologies
- Demonstrator for optical backplane connection
- Test bench for topological algorithms
- Test bench for future LHC clock distribution schemes
- Optical data sink for L1Calo modules
- Optical data source for purpose of self-test and stand-alone link tests
- ATCA Backplane zones 2 and 3 of the GOLD are used for real-time data transmission.

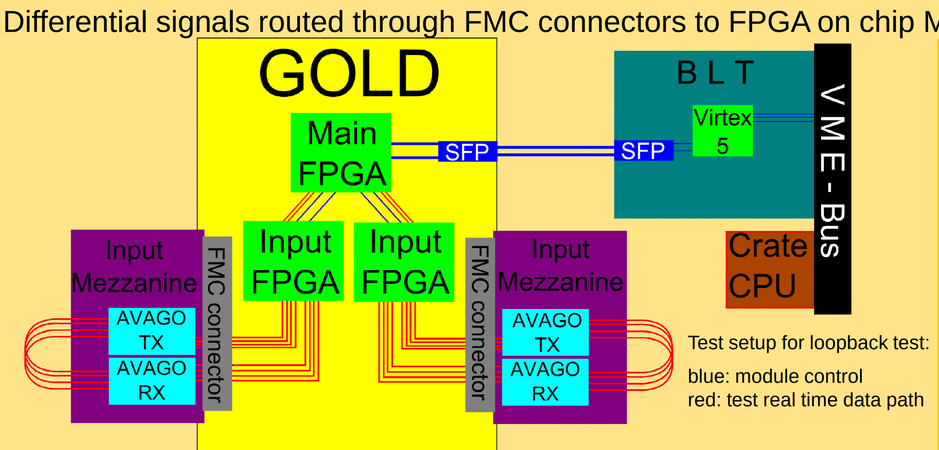


Block scheme of the GOLD components and RTDP

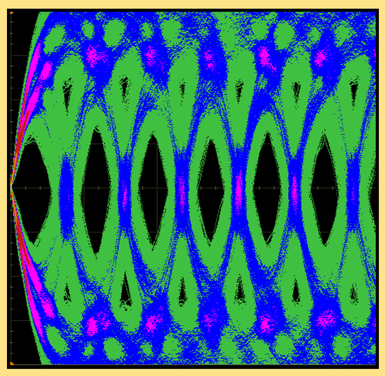


Clock Distribution, Control- and Real Time Data Path

- **Clocking:** All clocks coming from a special mezzanine
- Clock can be generated by an oscillator or use external clocks (plus jitter cleaner)
- Two clock trees support all 9 FPGAs with same clock for fabric
- High speed links get special clocks
- **Control:** GOLD is optically connected via SPF to 6U VME-busmodule(BLT) to get VME access
- **RTDP:** Input data routed via optical fibres through backplane zone1 (5x72channels)
- Opto-/electrical conversion with12-channel receivers on mezzanines
- Differential signals routed through FMC connectors to FPGA on chip MGTs



Test setup for loopback test:
blue: module control
red: test real time data path



Eye diagram at 6.4 Gb/s with old module(BLT)

Tests & Verification

Extensive tests to verify the functioning of the external hardware interfaces, board level connectivity and basic operation of components are planned:

- **Status**: PCB produced, component assembly finished next week, firmware development is ongoing
- **Boundary scan:** Interconnection test between FPGAs with JTAG boundary scan performed using GOEPEL electronics boundary scan software SYSTEMCASCON
- **Latency:** Verify simulated latency of algorithms and minimize latency of 6.4 Gb/s high speed links and input - main FPGA interconnection (1.2 Gb/s)
- **Bit Error Test (IBERT):** ChipScope Pro Serial I/O toolkit integrate debug of high-speed serial transceiver of Xilinx FPGAs. Measure until bit error rate < 10^{-15}
- **Transceiver fine tuning:** Combined test of opto-electro converter (AVAGO) connected to MGTs (in FPGA). Change parameters like equalization and pre-emphasis and measure eye diagram by swapping the sampling point or directly with oscilloscope(80 GSa/s, 32 GHz)
- **Real Time Data Path (RTDP) full chain:** Send data in loopback , run algorithms on received data and transmit result to other FPGA