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An FPGA based demonstrator for a topological processor in the future ATLAS L1-Calo trigger ("GOLD")

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The existing ATLAS trigger consists of three levels. The level 1 (L1) is an FPGAs based custom designed trigger, while the second
and third levels are software based.\\

The LHC machine plans to bring the beam energy to the nominal
value of 7 TeV and to increase the luminosity in the coming years.
The current L1 trigger system is therefore seriously challenged.\\
To cope with the resulting higher event rate, as part of the ATLAS trigger upgrade, a new electronics module is foreseen to be added in the L1-Calo electronics chain:
the topological processor.\\

Such processor is provided with fast optical I/O and large bandwidth capability, in order to use the information on the cluster position in space (i.e. jets in the calorimeters or muons in the muon detectors) and improve the purity of the L1 triggers streams by applying topological cuts within the latency budget.\\

In this talk, an overview of the adopted technological solutions and the R&D activities on the demonstrator ("GOLD") are presented.

Summary 500 words

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The GOLD" (Generic Opto Link Demonstrator) is a first technology demonstrator for the topological processor. It is designed in AdvancedTCA (ATCA) form factor and together with its mezzanine modules, it will populate three adjacent slots of a standard ATCA shelf. Backplane connection, however, is made to a single ATCA slot only. The mezzanine modules make use of industry standard connector types, but they are built inGOLD" specific PCB dimensions.\\

The Topological Processor within the L1Calo architecture is going to be a single processor crate equipped with one or several processor modules. The processor modules will either be identical copies with firmware adapted to the specific topologies to operate on.\\

The "GOLD" processing resources are partitioned into four input processors and a main processor. This is not a requirement, but a consequence of limitations on MGT link count and processing resources on currently available FPGAs. The aggregate input bandwidth is of 737Gb/s (payload) into the processors
(144 channels of up to 6.4Gb/s line rate). The requirements on processing resources depend on the physics algorithms and are not currently known.\\

The information transmitted comprised of the Region Of Interest (ROI) data that are currently transmitted to the 2nd level trigger. The ROI consist of a description of the position in space of an object (jet, e/m cluster, and tau) along with some qualifying
information. Data are transmitted on optical fibers, converted to electrical representation, and processed in FPGAs equipped with on-chip Multi-Gigabit Transceivers (MGT).\\

The ROI information on the cluster position in space (i.e. jets in the calorimeters or muons in the muon detectors) is the used to enhance the purity of the L1 triggers streams without deteriorating the efficiency and performance, by applying topological cuts.

Since the L1 architecture has to cope with a limited and fixed latency budget, the latency on chip-to-chip data transmission and to run the topological algorithms has to be minimized.\\

This talk will mostly focus on the adopted technological solutions. Results from tests performed on the first demonstrator and all possible issue emerged from the R&D activities are presented.\\

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