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The MEMDYN chip: a new circular memory prototype for a plannar pixel sensors readout IC

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A low-power and low-area circular memory has been designed in a 130 nm technology. This prototype aims to be integrated into a plannar pixel sensors readout 3D integrated circuit for the future ATLAS high luminosity upgrade.

Three types of memory cell have been designed: one with Typical transistors, an other with low-Vt transistors and the last one with custom enclosed transistors. The digital data is stored in parasitic capacitance between the gate and the source of a NMOS transistor.

Functionality and performance, before and after irradiation, will be shown.

Summary 500 words

The design and the measurements of a low-power and low-area circular memory will be presented.

The ATLAS Pixel project at LAL (Orsay) is involved in the design of a new pixel readout integrated circuit for the ATLAS Inner Detector for the future High Luminosity Upgrade. This R&D project aims to read out very small plannar pixel sensors with a 50 μm pitch. The Vertically Integrated Technology (3D) provided by Tezzaron and Global Foundries (Chartered) in 130 nm technology allow us to separate the analog and digital parts in two stacked tiers. Measurements of a prototype of the digital part will be shown.

The pixels being very small, the power consumption is a very important requirement to keep the power dissipation in a reasonable range (in a same range per area as the previous one for bigger pixels).

The MEMDYN circuit embeds three matrices of 50x50 μm² pixel divided in 6 columns and 41 rows. A circular memory has been implemented in each pixel which memorizes all the events up to L1 trigger acquisition.

Each circular memory is 120 depth allowing to keep data from all the Bunch Crossing during 3 us at 40 MHz, and so up to L1 trigger acquisition. Three microseconds (@ 40 MHz) after having been written, the memory cell is read: if the corresponding bunch crossing has been triggered the data is sent out of the matrix, otherwise the data is removed. Since the great majority of hits will not be triggered - in fact less than 2 % of hits will be triggered –the best way to minimize the power consumption is to minimize processing on all hits before triggering.

A new structure of cell memory has been designed in order to minimize the power dissipation and the area occupancy. The digital data is stored in parasitic capacitance between the gate and the source of a NMOS transistor. This structure allows to write data by connecting the write bus to the gate of the transistor, and to read the data by switching the drain to the read bus.

Three types of memory cell have been designed: one with Typical transistors, an other with low-Vt transistors and the last one with custom enclosed transistors. The measurement results will be presented: the storage time in regards to the leakage currents and the performances before and after irradiation.

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