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A CMOS 0.13 um Silicon Pixel Detector Readout ASIC for the PANDA experiment

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The ToPiX ASIC is a custom development for the hybrid pixel sensors of the PANDA experiment Micro Vertex Detector.
The ASIC will provide both the time and amplitude informations (via the Time over Threshold technique) of the incoming particle. ToPiX will consist of a matrix of 116x110 cells with a pixel size of 100x100 um2, the column readout logic and two 311 Mbit/s serializers.
A reduced scale prototype in CMOS 0.13 um has been designed and is currently under test. The prototype includes eight columns with the full cell analogue and digital circuitry and the end of column readout.

Summary 500 words

The PANDA experiment at the future FAIR facility under construction
near the GSI research center at Darmstadt, Germany, aims to the study of the antiproton-proton and antiproton-nucleus annihilation
reactions.
The Micro Vertex Detector (MVD) is the innermost part of the experiment and will consist of silicon pixel and silicon strip detectors to obtain precise tracking of all charged particles. Owing to the high track density (up to 6.1 MHz/cm2) and the absence of an hardware trigger signal, an ASIC based custom solution for the electronic readout of the pixel detector has been proposed. The ASIC, named ToPiX, will provide the time position of each hit with a resolution of 1.9 ns r.m.s. and a measure of the charge released with the Time over Threshold (ToT) technique. The ToT allows to achieve a wide dynamic range (up to 50 fC) with a quantization error of 58 e- r.m.s.
ToPiX will consist of a matrix of 116x110 cells with a pixel size 100x100 um2, thus covering a 1.32 cm2 active area. The pixel matrix is organized into double columns. Each double column has its separate data bus and readout logic. A data transmission logic multiplexes the data from the end of column control logic on three serializers. The master clock frequency is 155.52 MHz and the serializers will work at double rate, i.e. 311 Mb/s.
Detailed simulations based on the data from the physical simulations has been performed in order to prove the effectiveness of the architecture in the foreseen environment.
A reduced scale prototype in a CMOS 0.13 um technology has been designed and is currently under test. The prototype includes four columns made of 128 pixel cells, four columns of 32 cells and and the end of column readout with a 32 cells deep FIFO for each double column. The cells can be bump-bonded to a detector. Each cell embeds a charge amplifier with constant current feedback capacitor discharge, a comparator with per cell adjustable threshold via a D/A converter, 12-bits leading and trailing edge register for time and ToT measurement and a 12 bit configuration register. The simulated ToT gain is 200 ns/fC, with a noise floor of 200 e- r.m.d. and a quantization noise of 58 e- r.m.s.
The control logic has been designed in order to be SEU tolerant. Triple redundancy encoding and Hamming encoding have been used for the pixel cell logic and the end of column logic, respectively.
Differential SLVS I/O links have been used to interface the chip with the rest of the system. The ToPiX ASIC is foreseen to be connected with the GBT transceiver under development at CERN for data and slow control signal transmission.

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