Characterization of a commercial 65nm CMOS technology for SLHC applications

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Motivation

- Future vertex detectors for high energy physics experiments can benefit from modern deep submicron technologies
  - Scaling is necessary to improve the performances of pixel detectors
    - Smaller pixel sizes (pitch)
    - More “intelligence” in each pixel
- In general, the expected advantages in porting a front-end circuit to a more advanced technology include
  - A much more compact digital part (reduction in area of ~60% compared to 130nm technology)
  - Lower noise equivalent charge, due to the reduced capacitances associated with smaller pixels
- Studies on radiation hardness of the selected technology are needed
  - A set of test chips was designed, fabricated and tested to assess radiation hardness and functionality of both analog and digital test structures

Characterization strategy

- TID and SEU evaluation of 65 nm
  - Comparison with existing data on 130nm
  - Some data compared to 90 nm
- (Careful, different foundries!)

Drawbacks of 65 nm

- Higher gate leakage current

	65nm technology	130nm technology
Minimum gate length	60nm	120nm
Metal layers	10	8
Power supply	1.2 V - 1.0 V	1.5 V - 1.2 V
Gate leakage	350 pA/μm^2	20 pA/μm^2
Channel leakage (at minimum length)	211 pA/μm	400 pA/μm

- More stringent design rules: ELT transistors are not allowed, more difficult to achieve an optimal layout.
  - OPC rules: avoid jogs, zigzag, shapes like “L”, “U” or ring, …
- Deep submicron technologies are not optimized for analog designs
  - Smaller dynamic range due to the lower power supply reduces the possibilities to use some structures (such as cascoded stages). Multiple stages, with possible stability issues, are needed to achieve a high gain.
    - This problem is moreover aggravated by the lower output resistance of the MOSFETs which lowers the gain of the single stages.
- Higher cost of tape-out compared to older technologies
  - Strong push for 1st working silicon
  - Push for more IP re-usage?

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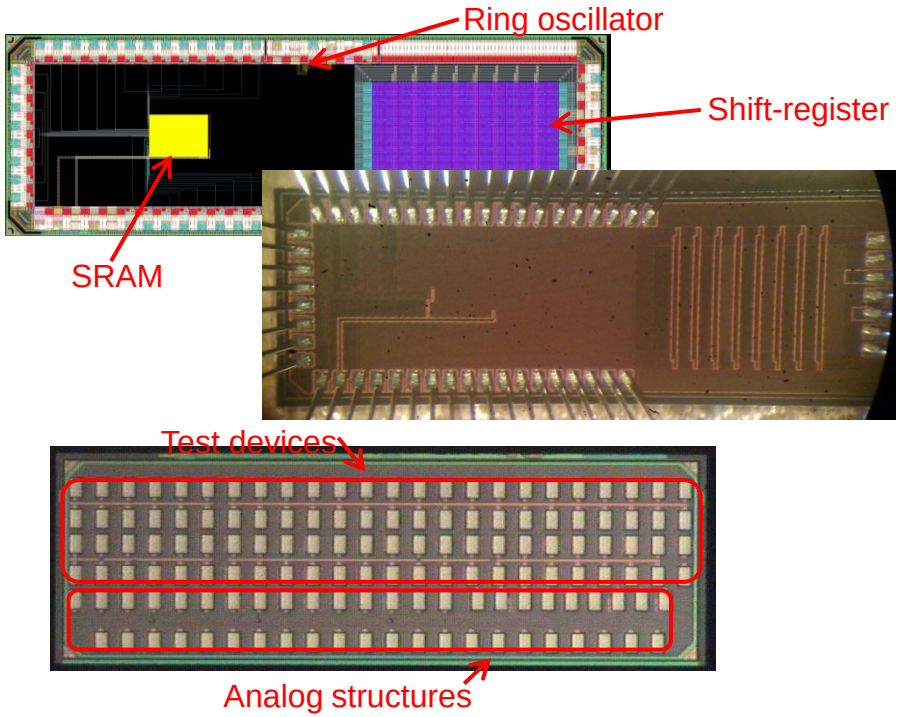
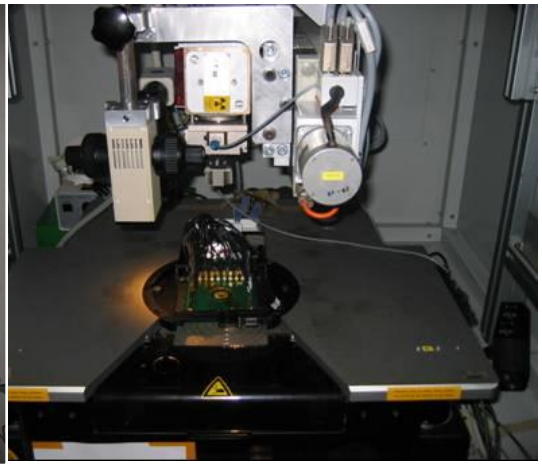
Test structures, measurement setup

- One chip with digital logic
  - Assembled with foundry standard cells, pads and IP blocks
  - Packaged, functional tests & irradiation measurements run on a custom test board
  - Shift-register
    - 64 kbit
  - Ring oscillator
    - 1025 inverters
  - SRAM (from foundry compiler)
    - 56 kbit
  - Irradiation up to 200 Mrad X-rays while operating
- One chip with devices and analog structures
  - Transistor devices
    - Irradiation & measurement at probe station, no bonding
  - Analog blocks
    - Preamplifier
    - Discriminator
    - Binary weighted DAC
    - Sub-binary radix DAC
  - Irradiation up to 200 Mrad X-rays under worst-case static bias

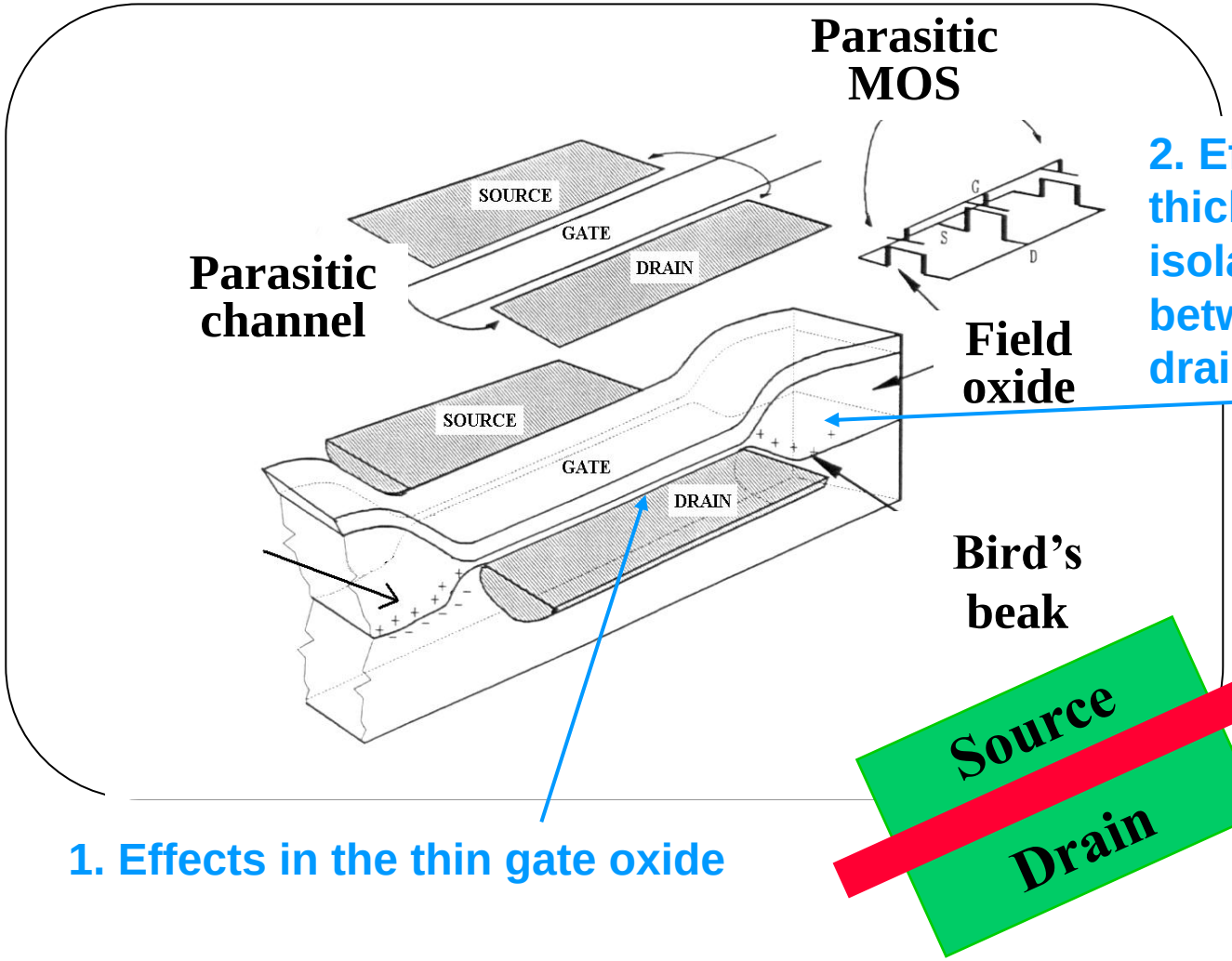




Technology flavour

- 65nm, low-power version
  - 1.2V supply for core
  - I/O supports 2.5 and 3.3V
  - HVMOS 5V-drain tolerant devices
- 6 metal levels (Cu)
  - inter-layer metal M2-M4
  - top metals M5-M6
- Last metal Al, redistribution layer (RDL)
  - 1.5 um or 2.8 um
  - used for pad (WB and bump), interconnection, laser fuses

TID effects on CMOS technology

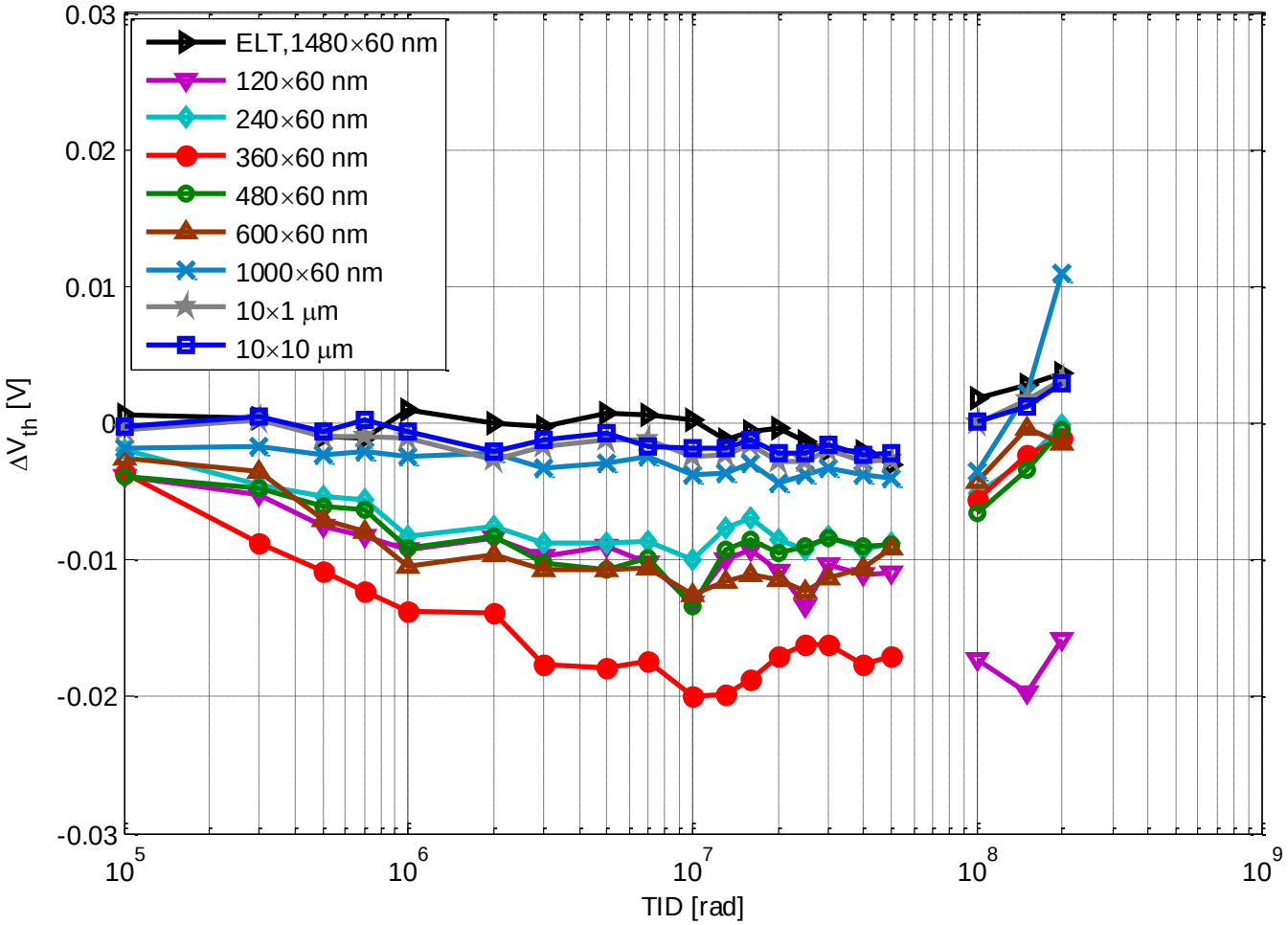


2. Effects in the thick lateral isolation oxide (STI) between source and drain of a transistor

1. Effects in the thin gate oxide

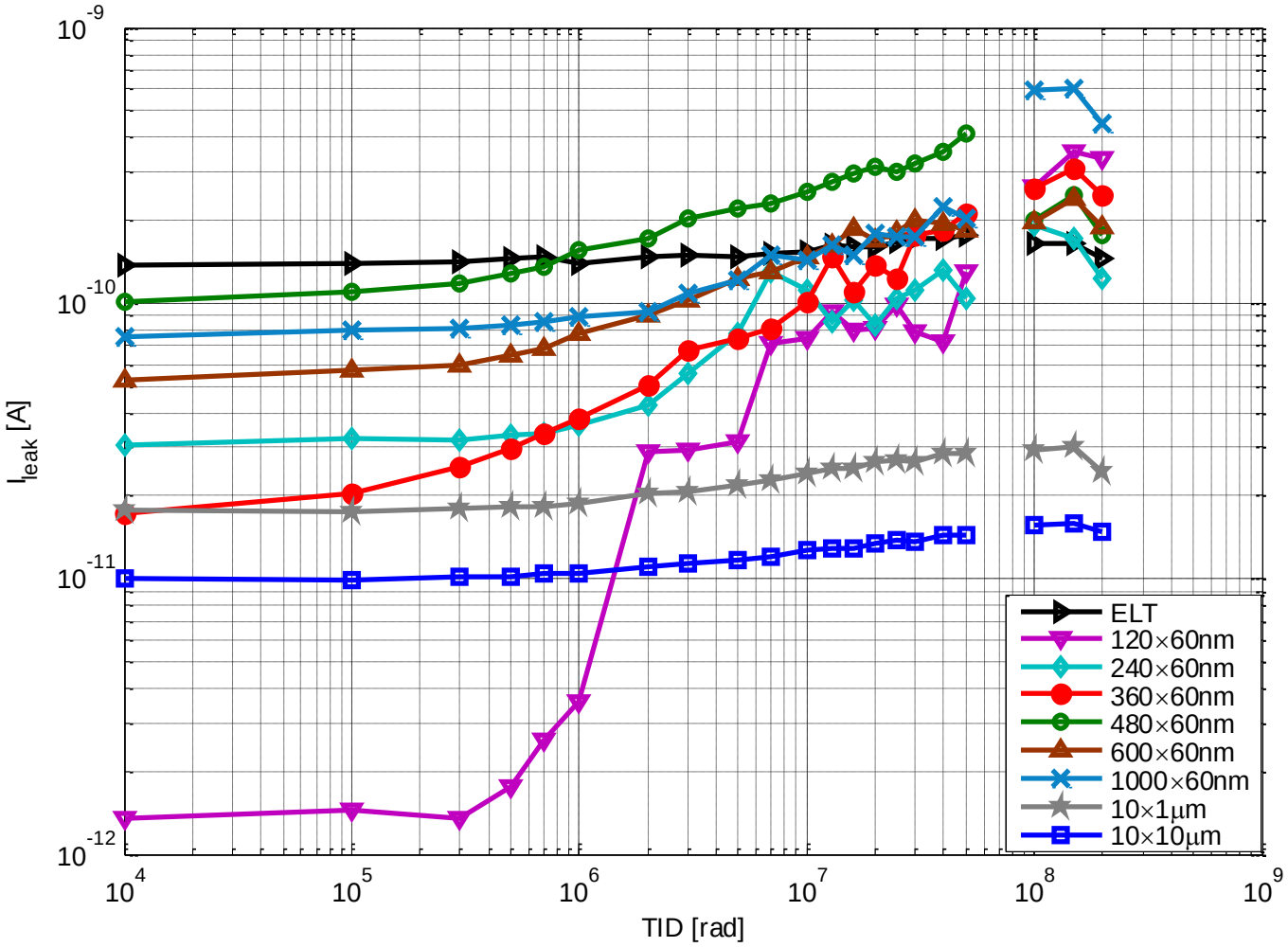
- Threshold voltage shift
- Leakage current

Core NMOS, threshold voltage shift



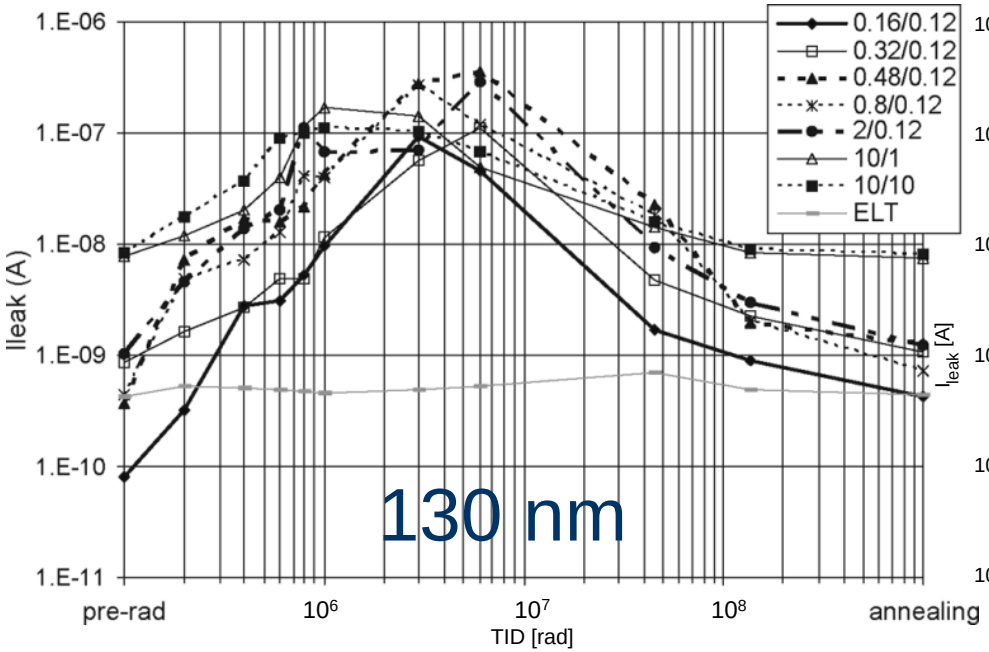
- Up to ~20mV shift for 200 Mrad
  - Some rebound effect visible for narrow devices
    - in 130nm: was 150mV
- At high doses Vth shift is positive for wide devices, negative for narrow devices
  - STI edge oxide traps considerable charge (RINCE)
- Subtreshold slope does not change significantly

Core NMOS, leakage current

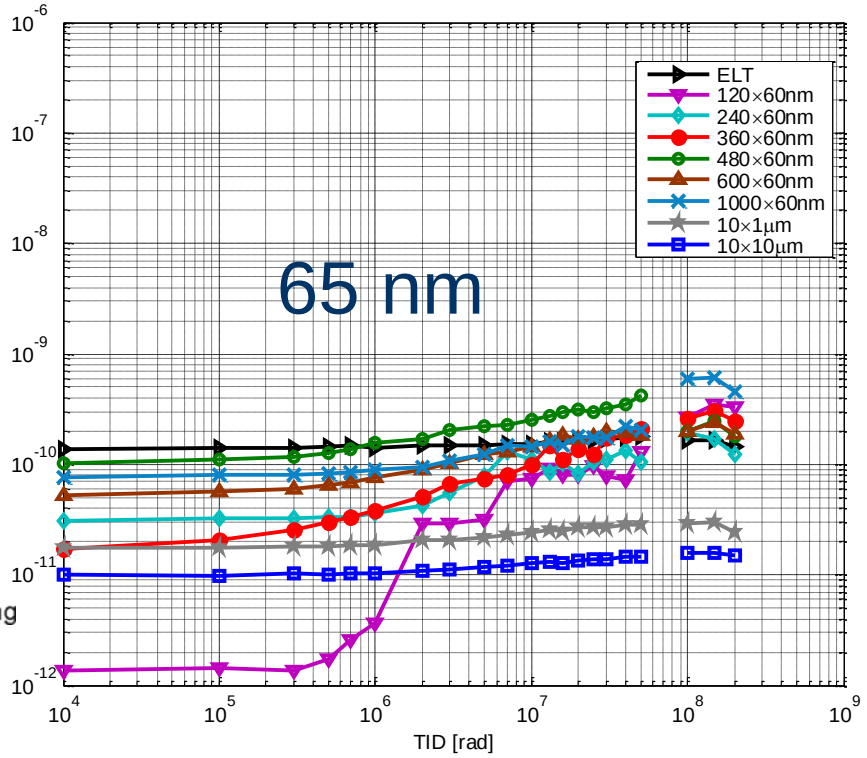


- Less than 10× increase in leakage for wide devices (W > 360nm)
- Narrow devices have up to 2.5 orders of magnitude increase
- Better performance with respect to 130nm

Core NMOS, leakage current

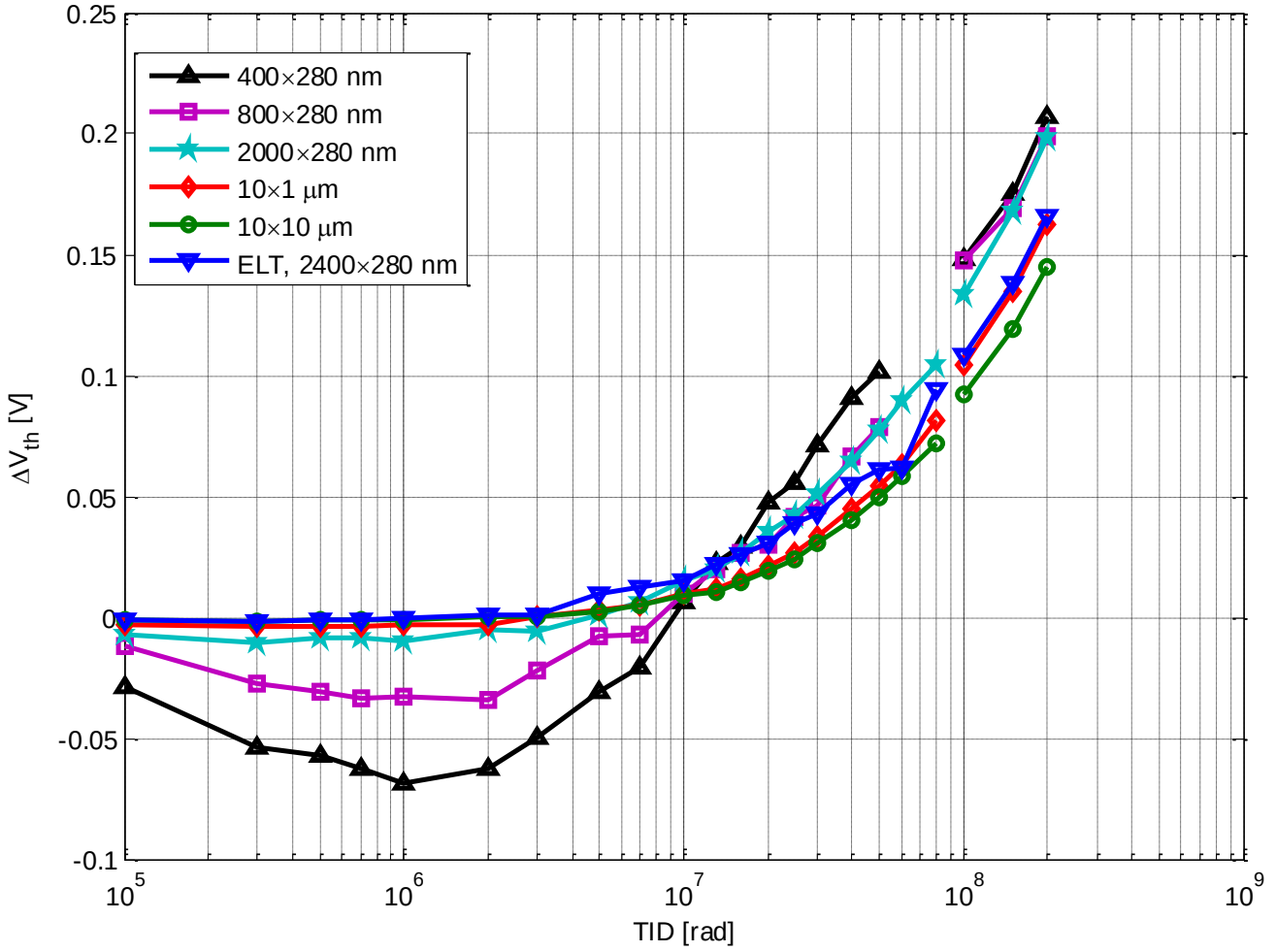


F.Faccio et al., "*Radiation-induced edge effects in deep submicron CMOS transistors*", IEEE Tr. Nucl. Sci. 2005



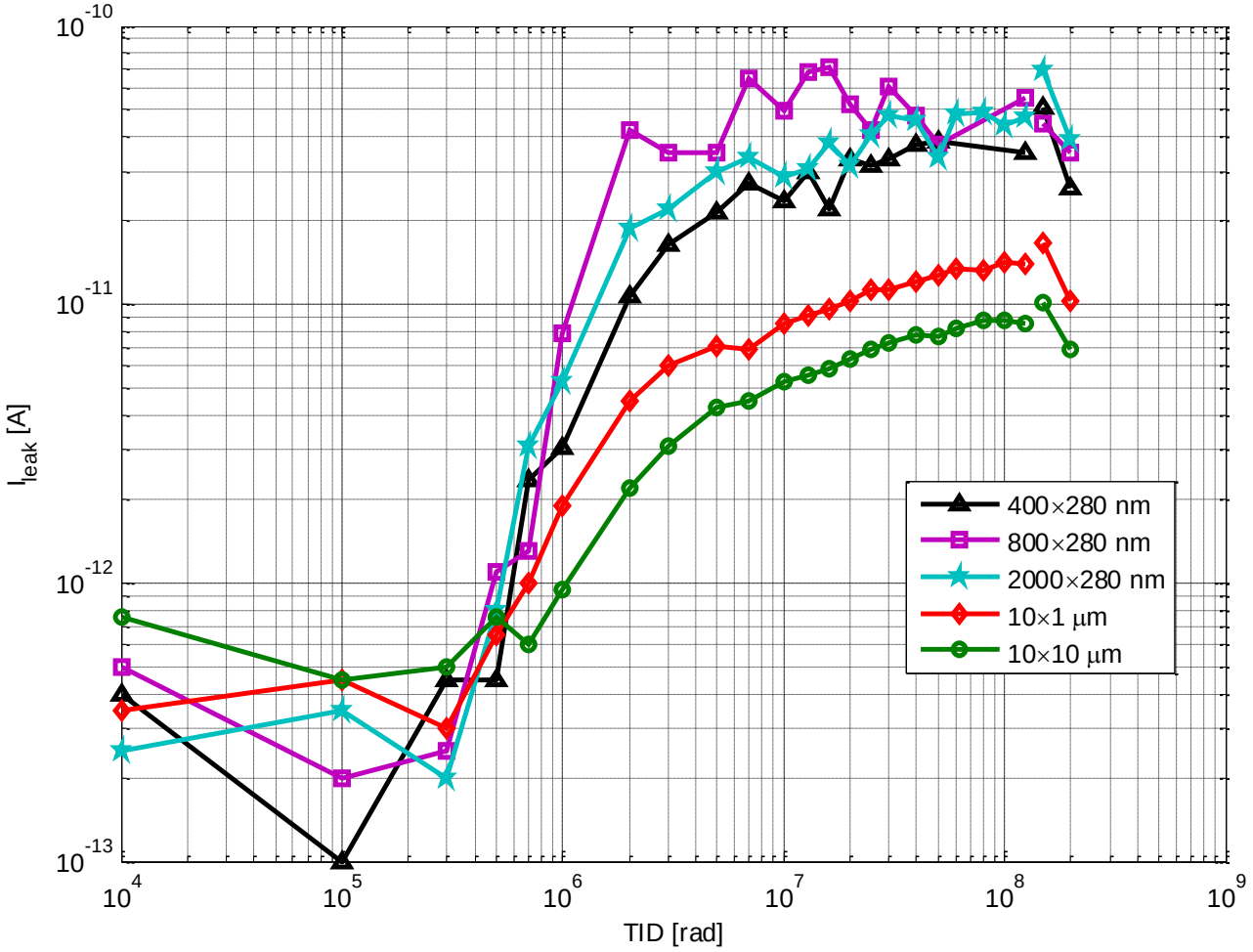
- 65nm has better performance with respect to 130nm: (**Plots are in the same scale**)
  - a rebound effect is visible in 130 nm:
  - all 130nm devices are peaking at ~100nA
  - Narrow devices increase I_{leak} by 3 orders of magnitude
  - I_{leak} is ~1nA @136 Mrad

I/O NMOS, threshold voltage shift



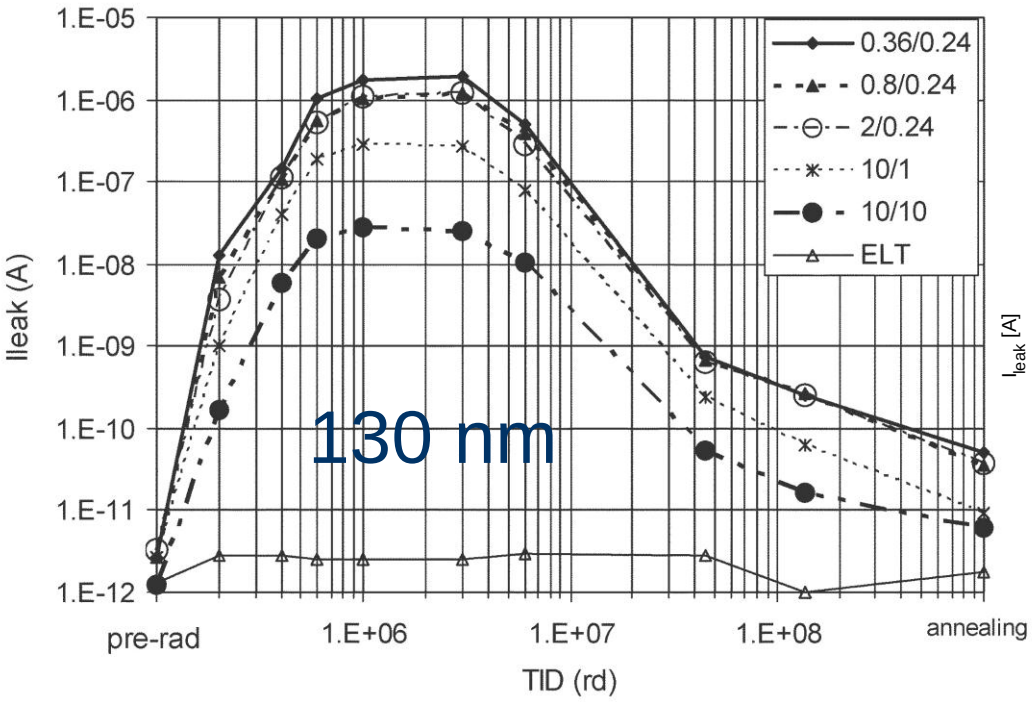
- Vth shift is positive at high doses
  - Up to ~200mV for 200 Mrad
    - $V_{th,0}$ is ~500mV
  - Interface states seem to dominate over trapped charge
  - Some rebound effect visible for narrow devices
- Bigger shift for narrow devices
- Similar to 130nm
  - max 170mV @136Mrad

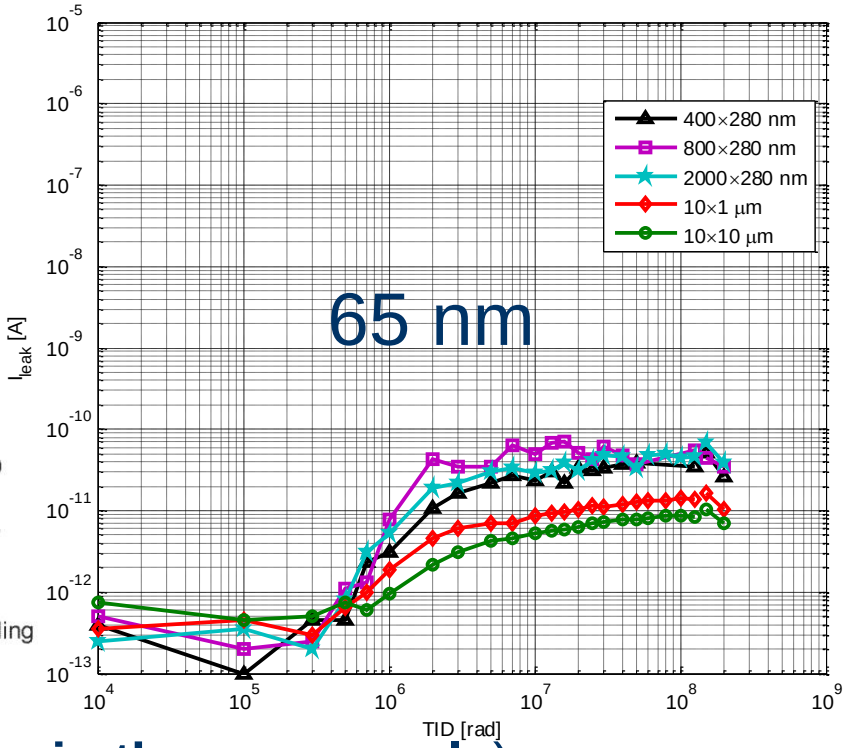
I/O NMOS, leakage current



- Increase in leakage by 2 orders of magnitude
  - Most around 1 Mrad, then saturates
  - No rebound within 200 Mrad
- Enclosed Layout Transistor (ELT) structure is advised

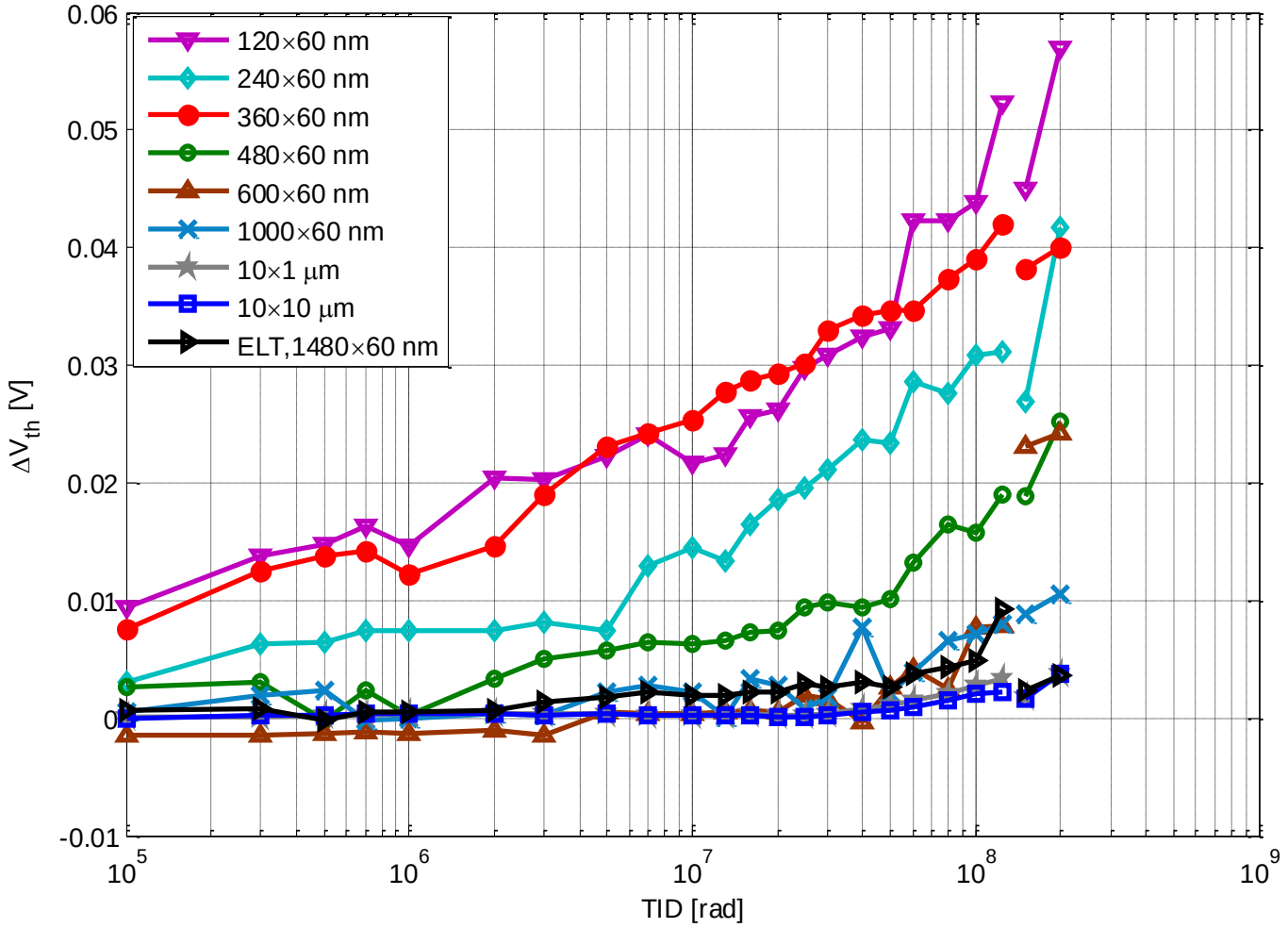
I/O NMOS, leakage current





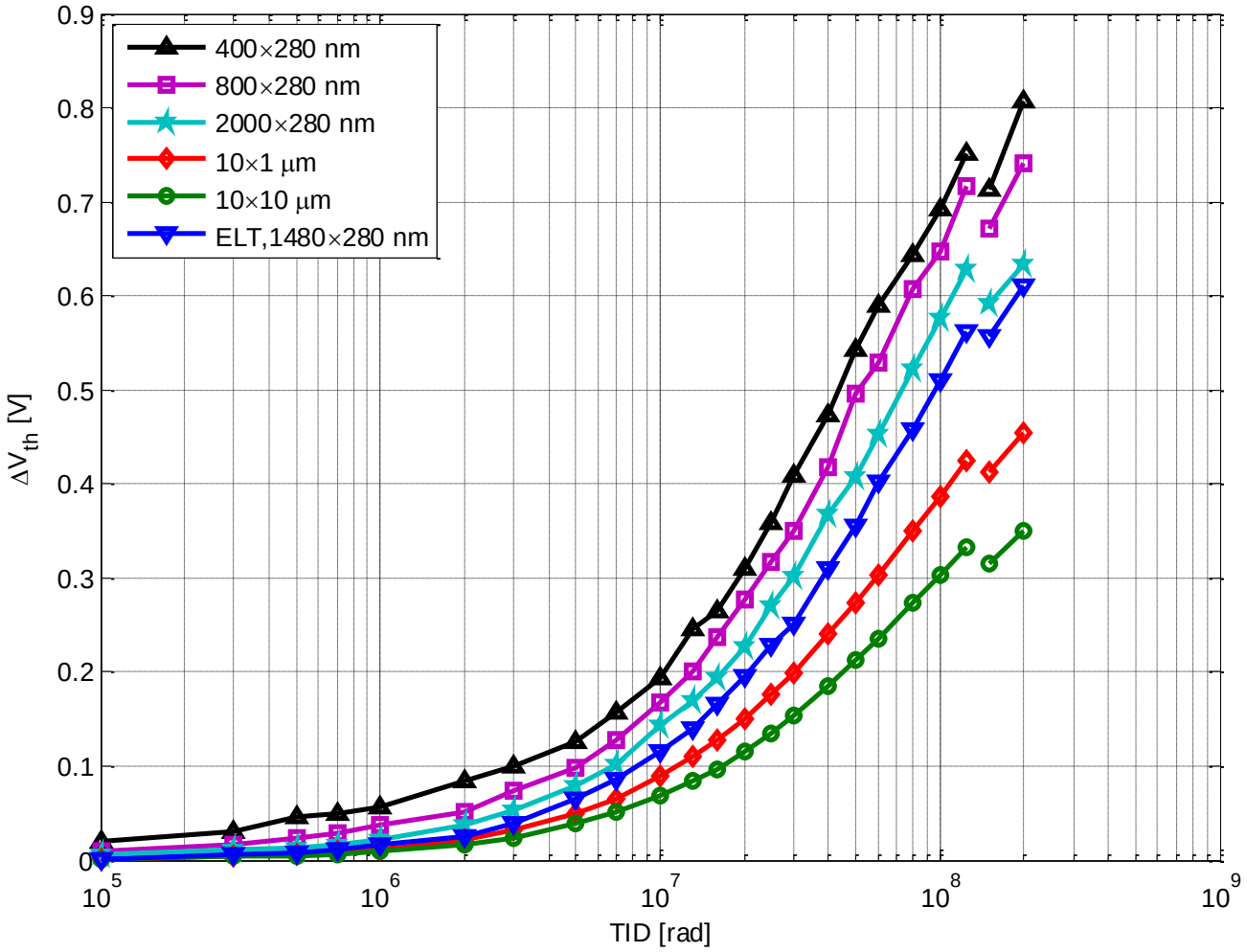
- Comparison with 130nm: (**Plots are in the same scale**)
  - devices had I_{leak} peaking at 1uA @ 2Mrad
    - had ~5-6 orders of magnitude increase
  - Similar current 100pA@136Mrad
  - 90 nm technology looks like 130nm (same foundry)

Core PMOS, threshold voltage shift



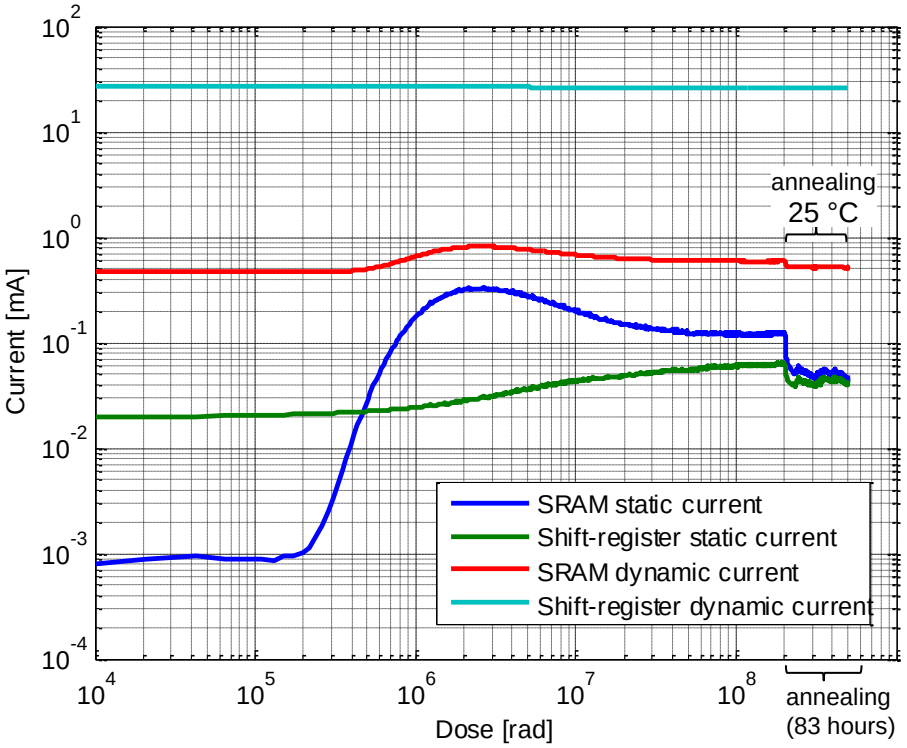
- PMOS Vth shift limited to 60 mV
  - trapped charge and interface states sum up
  - More evident for narrow devices
  - Less than 10mV for transistors with W>1um
- Compared to other technologies
  - Better performance than 130 nm
    - had up to 90mV @136Mrad
    - 30mV for wide devices
  - In a 90 nm tech we observed a similar effect: 70mV @ 200Mrad

I/O PMOS, threshold voltage shift



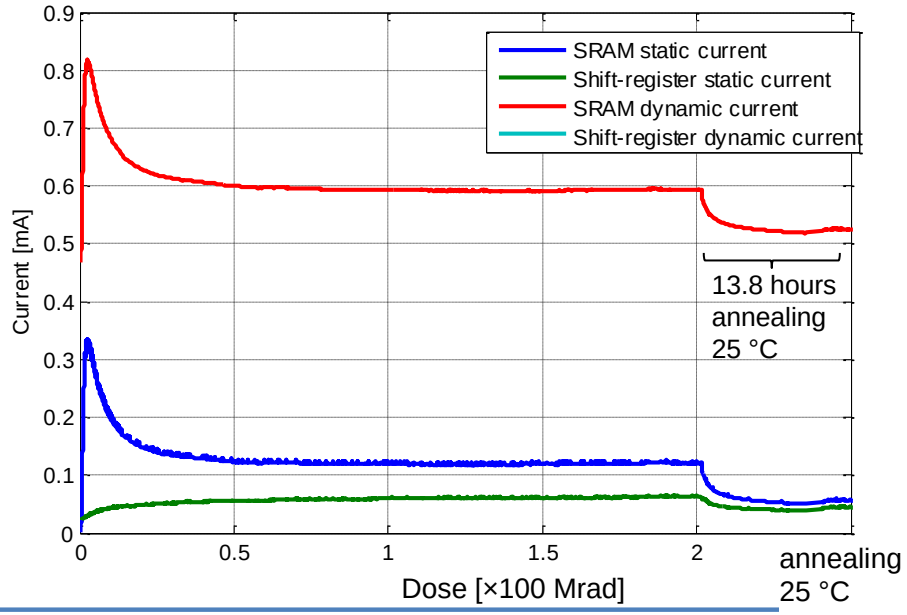
- Considerable shift of the threshold voltage
  - Up to 800 mV (+160%) for 200 Mrad
    - V_{th0} is ~550mV
  - More pronounced for narrow channel transistors
  - Devices turn off
    - Design must be oversized
- Worse performance than in 130nm
  - Had max 450mV shift @136Mrad
- Similar to 90 nm
  - Seen 600mV @200 Mrad

Digital test structures #1

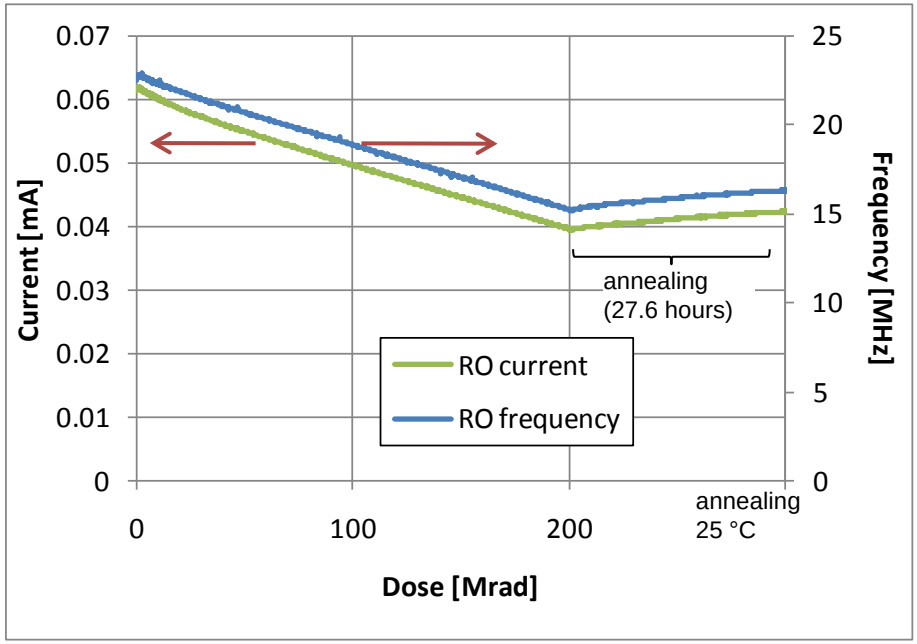


- Shift-register static current changes very little
  - Dynamic current practically constant (decrease!)
    - ~12.5 nW/MHz per D-FF
- Visible partial annealing effect at room temperature
  - Time constant ~ 1.5 hours

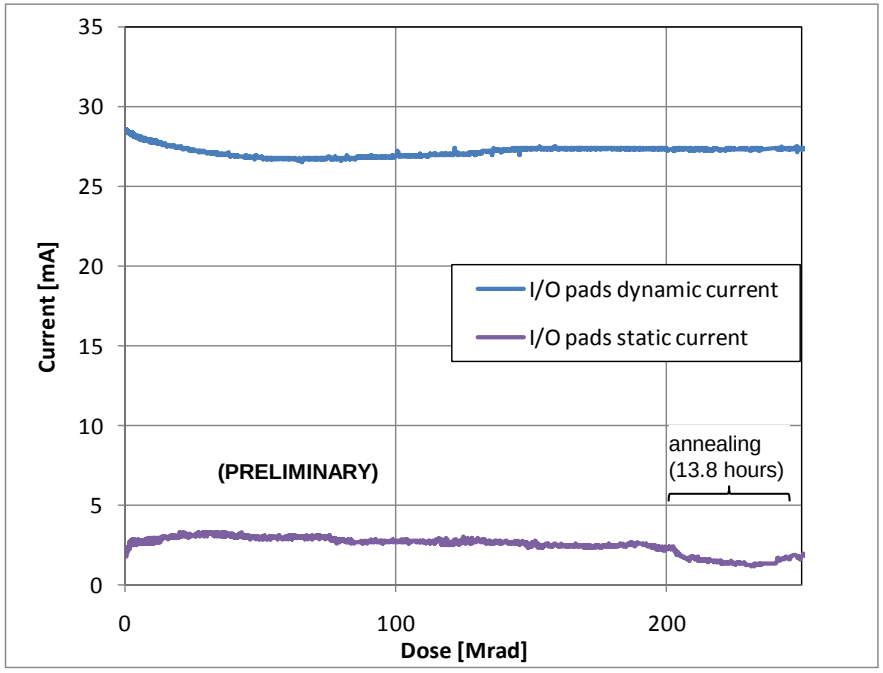
- Measured static and dynamic currents of SRAM and shift-register
  - Dynamic test run @ 30MHz
- SRAM static current increases by 300×
  - Dynamic current reflects this change with a small increase
  - Ultra-narrow devices are used in the SRAM from foundry (W=80nm)
  - Peak current at ~2-3 Mrad
    - Dependent on dose rate (?)



Digital test structures #2

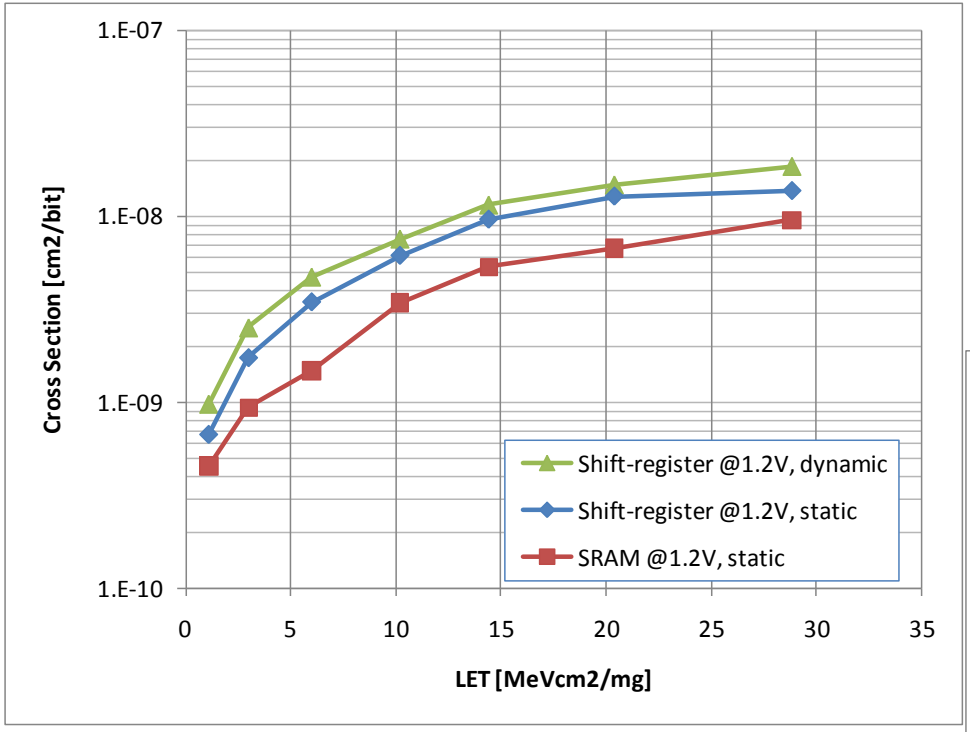


- Ring oscillator
  - Logic slows down with radiation (preliminary)
    - Must keep margin in digital design?
    - Annealing data must be taken!!!
  - Current and speed remain proportional
    - ~ 3 nW/MHz for 1 inverter
    - Speed range: 21 – 32 ps/inverter

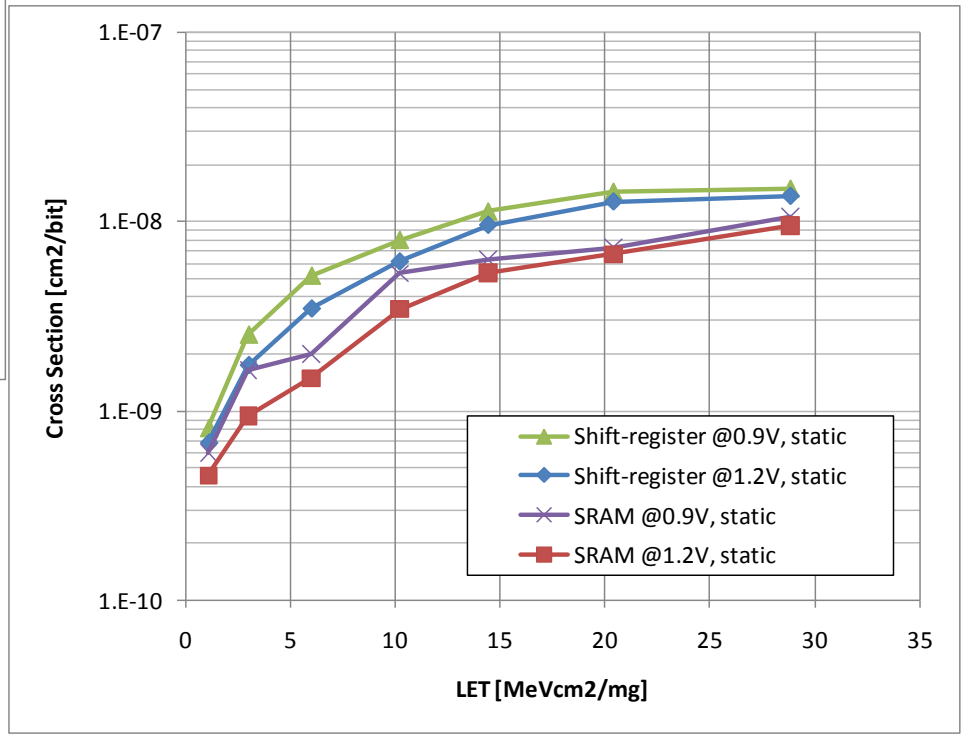


- Negligible changes in I/O pad currents (preliminary)
  - 39 I/O pads @2.5V supply

SEU test results – heavy ion beam



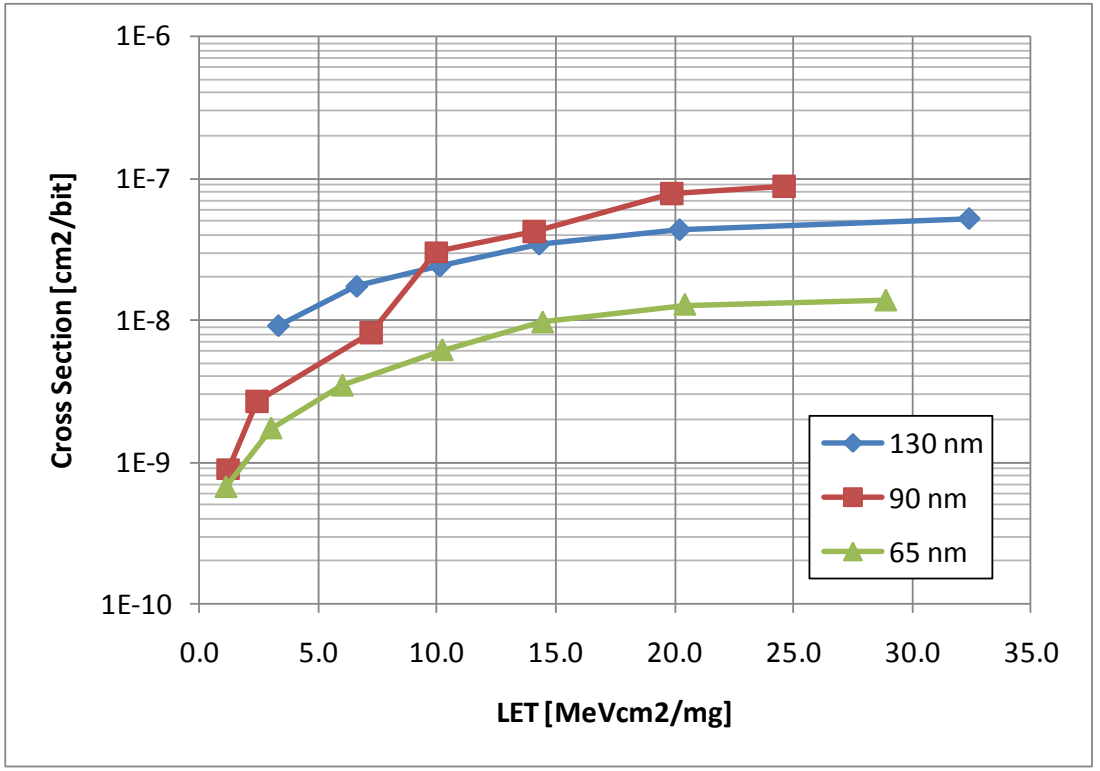
- No substantial differences between static test and dynamic test run at 30 MHz
- Evidence of 1 clock root SEU hit



- Max 1.7× increase in cross-section with reduced power supply voltage @ 0.9V

SEU test results, tech. comparison

- 65nm seems to saturate at a cross-section 3.4× smaller than 130nm
  - About proportional to 4× area reduction
- 90nm registers were custom-made (not standard cells)
  - Higher saturation cross-section though area is ½ of cell in 130 nm
- LET thresholds are less than 1.1 MeVcm2/mg for all technologies
- Note: SEU-robust cells are well below 10^{-10} cm^2/bit



Thank you…

- 65 nm demonstrates a better radiation hardness than previous generation technologies
  - TID is as good or better
  - SEU is better as sensitive areas are smaller
    - But beware in using more logic in chips
- Analog circuits results will be presented in a future publication
  - So far, so good…
- Current work & future plans
  - Measurements on FOXFETs, devices with varying L, HVMOS, highVt devices …
  - Annealing effects
  - X-ray irradiation @ low temperature (-30 °C)