Characterization of a commercial 65nm CMOS technology for SLHC applications

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Motivation

- Future vertex detectors for high energy physics experiments can benefit from modern deep submicron technologies
  - Scaling is necessary to improve the performances of pixel detectors
    - Smaller pixel sizes (pitch)
    - More “intelligence” in each pixel
- In general, the expected advantages in porting a front-end circuit to a more advanced technology include
  - A much more compact digital part (reduction in area of ~60% compared to 130nm technology)
  - Lower noise equivalent charge, due to the reduced capacitances associated with smaller pixels
- Studies on radiation hardness of the selected technology are needed
  - A set of test chips was designed, fabricated and tested to assess radiation hardness and functionality of both analog and digital test structures
Characterization strategy

- TID and SEU evaluation of 65 nm
  - Comparison with existing data on 130nm
  - Some data compared to 90 nm
- (Careful, different foundries!)
Drawbacks of 65 nm

- Higher gate leakage current

<table>
<thead>
<tr>
<th></th>
<th>65nm technology</th>
<th>130nm technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum gate length</td>
<td>60nm</td>
<td>120nm</td>
</tr>
<tr>
<td>Metal layers</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>Power supply</td>
<td>1.2 V - 1.0 V</td>
<td>1.5 V - 1.2 V</td>
</tr>
<tr>
<td>Gate leakage</td>
<td>350 pA/μm²</td>
<td>20 pA/μm²</td>
</tr>
<tr>
<td>Channel leakage (at minimum length)</td>
<td>211 pA/μm</td>
<td>400 pA/μm</td>
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</table>

- More stringent design rules: ELT transistors are not allowed, more difficult to achieve an optimal layout.
  - OPC rules: avoid jogs, zigzag, shapes like “L”, “U” or ring, …

- Deep submicron technologies are not optimized for analog designs
  - Smaller dynamic range due to the lower power supply reduces the possibilities to use some structures (such as cascoded stages). Multiple stages, with possible stability issues, are needed to achieve a high gain.
  - This problem is moreover aggravated by the lower output resistance of the MOSFETs which lowers the gain of the single stages.

- Higher cost of tape-out compared to older technologies
  - Strong push for 1st working silicon
  - Push for more IP re-usage?
Test structures, measurement setup

- One chip with digital logic
  - Assembled with foundry standard cells, pads and IP blocks
  - Packaged, functional tests & irradiation measurements run on a custom test board
    - Shift-register
      - 64 kbit
    - Ring oscillator
      - 1025 inverters
    - SRAM (from foundry compiler)
      - 56 kbit
    - Irradiation up to 200 Mrad X-rays while operating

- One chip with devices and analog structures
  - Transistor devices
    - Irradiation & measurement at probe station, no bonding
  - Analog blocks
    - Preampifier
    - Discriminator
    - Binary weighted DAC
    - Sub-binary radix DAC
  - Irradiation up to 200 Mrad X-rays under worst-case static bias
Technology flavour

- 65nm, low-power version
  - 1.2V supply for core
  - I/O supports 2.5 and 3.3V
  - HVMOS 5V-drain tolerant devices

- 6 metal levels (Cu)
  - inter-layer metal  M2-M4
  - top metals M5-M6

- Last metal Al, redistribution layer (RDL)
  - 1.5 um or 2.8 um
  - used for pad (WB and bump), interconnection, laser fuses
TID effects on CMOS technology

1. Effects in the thin gate oxide
   - Parasitic channel
   - Threshold voltage shift
   - Leakage current

2. Effects in the thick lateral isolation oxide (STI) between source and drain of a transistor
   - Bird’s beak
   - Threshold voltage shift
   - Leakage current
Up to ~20mV shift for 200 Mrad
- Some rebound effect visible for narrow devices
- In 130nm: was 150mV

At high doses, Vth shift is positive for wide devices, negative for narrow devices
- STI edge oxide traps considerable charge (RINCE)

Subthreshold slope does not change significantly
- Less than $10 \times$ increase in leakage for wide devices ($W > 360 \text{nm}$)
- Narrow devices have up to 2.5 orders of magnitude increase
- Better performance with respect to 130nm
Core NMOS, leakage current

65nm has better performance with respect to 130nm: (Plots are in the same scale)
- a rebound effect is visible in 130 nm:
- all 130nm devices are peaking at ~100nA
- Narrow devices increase $I_{\text{leak}}$ by 3 orders of magnitude
- $I_{\text{leak}}$ is ~1nA @136 Mrad

I/O NMOS, threshold voltage shift

- $V_{th}$ shift is positive at high doses
  - Up to ~200mV for 200 Mrad
  - $V_{th,0}$ is ~500mV
  - Interface states seem to dominate over trapped charge
  - Some rebound effect visible for narrow devices

- Bigger shift for narrow devices

- Similar to 130nm
  - max 170mV @136Mrad
**I/O NMOS, leakage current**

- Increase in leakage by 2 orders of magnitude
  - Most around 1 Mrad, then saturates
  - No rebound within 200 Mrad

- Enclosed Layout Transistor (ELT) structure is advised

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- $I_{\text{leak}}$ [A]

- TID [rad]

- $400 \times 280$ nm
- $800 \times 280$ nm
- $2000 \times 280$ nm
- $10 \times 1 \mu m$
- $10 \times 10 \mu m$
I/O NMOS, leakage current

Comparison with 130nm: (Plots are in the same scale)
- devices had $I_{\text{leak}}$ peaking at 1uA @ 2Mrad
  - had ~5-6 orders of magnitude increase
- Similar current 100pA@136Mrad
- 90 nm technology looks like 130nm (same foundry)
Core PMOS, threshold voltage shift

- PMOS Vth shift limited to 60 mV
  - Trapped charge and interface states sum up
  - More evident for narrow devices
  - Less than 10mV for transistors with W>1µm

- Compared to other technologies
  - Better performance than 130 nm
    - Had up to 90mV @136Mrad
    - 30mV for wide devices
  - In a 90 nm tech we observed a similar effect: 70mV @ 200Mrad
Considerable shift of the threshold voltage
- Up to 800 mV (+160%) for 200 Mrad
  - $V_{th0}$ is ~550mV
- More pronounced for narrow channel transistors
- Devices turn off
- Design must be oversized

Worse performance than in 130nm
- Had max 450mV shift @136Mrad

Similar to 90 nm
- Seen 600mV @200 Mrad
Measured static and dynamic currents of SRAM and shift-register
- Dynamic test run @ 30MHz
- SRAM static current increases by 300×
  - Dynamic current reflects this change with a small increase
  - Ultra-narrow devices are used in the SRAM from foundry (W=80nm)
  - Peak current at ~2-3 Mrad
    - Dependent on dose rate (?)

Shift-register static current changes very little
- Dynamic current practically constant (decrease!)
  - ~12.5 nW/MHz per D-FF

Visible partial annealing effect at room temperature
- Time constant ~ 1.5 hours

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<thead>
<tr>
<th>Dose [rad]</th>
<th>Current [mA]</th>
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<tbody>
<tr>
<td>10^4</td>
<td>10^-4</td>
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<tr>
<td>10^5</td>
<td>10^-3</td>
</tr>
<tr>
<td>10^6</td>
<td>10^-2</td>
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<tr>
<td>10^7</td>
<td>10^-1</td>
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<tr>
<td>10^8</td>
<td>10^0</td>
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<table>
<thead>
<tr>
<th>Dose [×100 Mrad]</th>
<th>Current [mA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0.5</td>
<td>0.1</td>
</tr>
<tr>
<td>1</td>
<td>0.2</td>
</tr>
<tr>
<td>1.5</td>
<td>0.3</td>
</tr>
<tr>
<td>2</td>
<td>0.4</td>
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</tbody>
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Annealing 25 °C
13.8 hours

Annealing (83 hours)
Digital test structures #2

- **Ring oscillator**
  - Logic slows down with radiation (preliminary)
  - Must keep margin in digital design?
  - Annealing data must be taken!!!
  - Current and speed remain proportional
    - ~ 3 nW/MHz for 1 inverter
    - Speed range: 21 – 32 ps/inverter

- Negligible changes in I/O pad currents (preliminary)
  - 39 I/O pads @2.5V supply
SEU test results – heavy ion beam

- No substantial differences between static test and dynamic test run at 30 MHz
- Evidence of 1 clock root SEU hit

Max $1.7 \times$ increase in cross-section with reduced power supply voltage @ 0.9V
- 65nm seems to saturate at a cross-section $3.4 \times$ smaller than 130nm
  - About proportional to $4 \times$ area reduction
- 90nm registers were custom-made (not standard cells)
  - Higher saturation cross-section though area is $\frac{1}{2}$ of cell in 130 nm
- LET thresholds are less than 1.1 MeVcm$^2$/mg for all technologies
- Note: SEU-robust cells are well below $10^{-10}$ cm$^2$/bit
Thank you…

- 65 nm demonstrates a better radiation hardness than previous generation technologies
  - TID is as good or better
  - SEU is better as sensitive areas are smaller
    - But beware in using more logic in chips

- Analog circuits results will be presented in a future publication
  - So far, so good…

- Current work & future plans
  - Measurements on FOXFETs, devices with varying L, HVMOS, highVt devices …
  - Annealing effects
  - X-ray irradiation @ low temperature (-30 °C)