

## Characterization of a commercial 65nm CMOS technology for SLHC applications.

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The radiation characteristics with respect to Total Ionizing Dose (TID) of a 65 nm CMOS technology has been investigated. Single transistor structures of a variety of dimensions and several basic circuits were designed and fabricated. The circuits include a 64-kbit shift-register, a 9-kbit SRAM, a ring-oscillator, a low noise preamplifier, a low-power discriminator and two 6-bit DACs with different architectures to compare matching properties at this node. The test chips were irradiated up to 100 Mrad with an X-ray beam and the corresponding threshold shifts and leakage currents measured.

### Summary 500 words

Most of the microelectronics components developed for the first generation of LHC have been designed and developed using a commercial 250 nm CMOS technology with special layout techniques (enclosed transistors and guard-rings), with a considerable improvement over previous technologies in terms of radiation hardness, cost and performance. A second generation of designs for instrumentation for upgraded LHC detectors uses a 130 nm CMOS technology, which offers significant advantages in terms of density and power dissipation over the previous technology, especially as it does not require enclosed transistor layouts. Demand for ever smaller pixels, faster serializers and lower power in digital circuits justifies a full evaluation of a new 65 nm low-power technology which is expected to bring further benefits to high volume (at least on the HEP scale) designs.

The chosen 65 nm low-power CMOS technology was developed for logic and mixed-signal and RF circuits, and allows multiple supply voltages for core and I/O. Its nominal supply voltage is 1.2 V and it features a high-resistivity epitaxial substrate process, shallow trench isolation (STI), two gate oxide options (for 1.2 and 2.5 V operation), nickel-silicided low-resistance n+ and p+ polysilicon and diffusion areas. nMOS and pMOS are available with several different threshold values. High-voltage 5V-drain-tolerant devices are optional. The back-end offers 3 to 9 copper metal layers for interconnection plus 1 top aluminium layer for wirebond/flip-chip pad, pad redistribution layer and laser fuses. Options for metal-insulator-metal capacitors and ultra-thick-metal high-Q inductors are available. Low-k dielectric is used for thin metal connections.

Previous investigation of similar technologies in the 130nm node had shown significant differences in radiation characteristics that were attributed to fine details in the fabrication of critical process steps (gate oxides, STI etc.). The investigation on at least one example of this technology is intended to clarify similar issues on this lithography node.

The test chips contain digital and analog prototype circuits, namely a 64-kbit shift-register using standard cells from the foundry, a 9-kbit SRAM, a 1025 elements ring-oscillator, a preamplifier for pixel sensors with a 30 ns rise time and a minimum 500ns shaping time, a low-power discriminator (~5 uW), a binary-weighted 6-bit DAC and a sub-binary radix DAC with an effective 6-bit precision.

In order to examine the devices' behaviour in the environment of high energy physics experiments, irradiation of some devices was performed using CERN's in-house X-ray generator. The ambient temperature during irradiation was 25 °C and different dose rates were applied. The devices were biased and driven with nominal operation conditions during irradiation. Circuit performance was monitored during and after irradiation as well as after annealing periods. Test results will be presented.

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