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Low Noise Front End ASIC with Current Mode Active Cooled Termination for the Upgrade of the LHCb Calorimeter

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An integrated circuit for the Upgrade of the LHCb Calorimeter front end electronics is presented. The circuit is based on a two fully differential interleaved channel with a first amplifier stage and a switched integrator. It offers an electronically cooled input termination at the input to achieve the stringent noise requirements. Compared to previous designs, its novelty relies in the use of two current feedback loops used to decrease and control the input impedance of a common base transistor. The selected technology corresponds to AMS SiGe BiCMOS 0.35um. Measured noise is below 1 LSB (12 bit scale) and linearity absolute relative error below 1%.

Summary 500 words

The LHCb is one of four large experiments of the Large Hadron Collider (LHC) based at the CERN laboratory near Geneva. It has already been taking data and it is expected to collect an integrated luminosity which will largely cover its proposed physics program in the following five years. However, in order to distinguish among models of new physics, a large increase in data rate is needed. LHCb collaboration intends to upgrade the detector during the planned long LHC shutdown in 2016.

We consider here the RD work for the upgrade of the front end electronics of the calorimeter subdetectors. The analogue signal processing in the present ECAL Front End (FE) board is mostly performed by a shaper ASIC that integrates the photomultiplier (PMT) pulse, which has been clipped at the PMT base. The PMT is located at the detector; the signal is transmitted through a 12m 50Ω coaxial cable to the FE board located in the crates at the calorimeter platform.

The PMT gain has to be decreased by a factor 5 in order to tolerate the increase in luminosity, and avoid ageing problems. Therefore, the preamplifier input equivalent noise must be decreased; the total input referred noise voltage of the front should be smaller than 1nV/√Hz. Consequently, a 50Ω termination resistor is not acceptable. An ASIC development was proposed because the FE board has 32 channels and a transistor level approach was required for any active termination scheme.

The presented implementation of the ASIC includes two alternated switched signal paths where the input current is first amplified and converted to differential signaling in order to be integrated through a fully differential amplifier with capacitive feedback. The solution is to alternate every 25 ns between two integrators and to reset one integrator when the other one is active. A fully differential signal processing is adopted in order to minimize the impact of common mode noise, which is important in a switched system.

The input amplifier presents an electronically cooled termination in a novel current mode scheme. It can be defined as a "super common base"input stage with double feedback. Two current feedback loops are used to decrease and control the input impedance of a common base stage with emitter degeneration to provide additional transconductance linearization.

The current mode implementation has several advantages with respect to previous designs: low voltage, DC coupling (no external components or additional pads), all nodes have low impedance (less prone to pick up noise), and ESD robustness is improved.

The switched integrator is based in a fully differential operational amplifier with > 500 MHz GBW and > 65 deg phase margin for moderate capacitive loads (below 15 pF).

A Track-and-Hold for a 12-bit ADC is added at each channel. It is realized in flip around topology with an operational transimpedance amplifier. It also includes a bootstrap circuit and a bottom-plate sampling network to optimize linearity.

A first prototype (called ICECAL) of input stage of the chip including preamplifier and switched integrators has been designed in Austriamicrosystems 0.35 um SiGe BiCMOS technology, with 3,3 V power supply.

Key tests have been performed on this prototype. The input impedance control by current feedback is properly working; the input reflection coefficient is less than 1% for full dynamic range. Also, test results limit the noise to 585 μV when Correlated Double Sampling (CDS) with a 50 ns delay is applied. CDS simulation noise is 480 uV rms. Linearity measurements for 12 chips offer a better linearity absolute relative error than 1% for the

full signal range.

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