The FE-I4 Pixel Readout System-on-Chip Resubmission to accommodate the Fast Track IBL plans

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Outline

• Introduction (FEI4-A)
• Resubmission project (FEI4-B)
• Design Effort
• Evaluation and Testing
• Conclusion and next steps
FEI4 Project

Insertable B-Layer (IBL) Application

- Designed for higher LHC luminosity
- Main functional part of readout core
- Array made of 80 analog columns & 40 digital double columns with 336 rows
- Direct and Shunted LDO powering scheme
- Sensors must be DC coupled to the top of FE-I4 with negative charge collection

 Existing B-layer

 IBL mounted on new beam pipe

 FE-I4 modules

 Carbon fiber facing

 Coolant tube

 Multi-layer cable with pre-bent tabs and connectors

 Carbon foam

 20mm x 19mm

 Main functional part of readout core
### FE-I4 Basic Function and Spec

- Remember the time and the charge of all hit pixels for the latency of ATLAS Level 1 trigger
- A trigger signal can select a particular 25ns time slice for persistent storage and transmission of all hits in that time window

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel array size</td>
<td>80x336</td>
</tr>
<tr>
<td>Pixel size</td>
<td>50x250 um²</td>
</tr>
<tr>
<td>Maximum charge</td>
<td>100 000 e⁻</td>
</tr>
<tr>
<td>Hit trigger association resolution</td>
<td>25 ns</td>
</tr>
<tr>
<td>Same pixel two-hit discrimination (time)</td>
<td>400 ns</td>
</tr>
<tr>
<td>Tuned threshold dispersion</td>
<td>&lt; 100 e⁻</td>
</tr>
<tr>
<td>Charge resolution</td>
<td>4 bits</td>
</tr>
<tr>
<td>ADC method</td>
<td>TOT</td>
</tr>
<tr>
<td>Radiation tolerance</td>
<td>250 MRad</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>-40° C to 60° C</td>
</tr>
<tr>
<td>Average hit rate with &lt; 1% data loss</td>
<td>400 MHz/cm²</td>
</tr>
<tr>
<td>Readout initiation</td>
<td>Trigger command</td>
</tr>
<tr>
<td>Max number of consecutive triggers</td>
<td>16</td>
</tr>
<tr>
<td>Trigger latency (max)</td>
<td>6.4 μs</td>
</tr>
<tr>
<td>Maximum sustained trigger rate</td>
<td>200 kHz</td>
</tr>
<tr>
<td>External clock input (nominal)</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Single serial command input (nominal)</td>
<td>40 Mb/s</td>
</tr>
<tr>
<td>Single serial data output (nominal)</td>
<td>160 Mb/s</td>
</tr>
<tr>
<td>Output data encoding</td>
<td>8b/10b</td>
</tr>
<tr>
<td>I/O signals</td>
<td>LVDS</td>
</tr>
</tbody>
</table>

![Target hit rate for FE-I4: 50KHz / pixel (400MHz/cm²) threshold]

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Vladimir Zivkovic

Vienna, 27-09-2011
FEI4-A Architecture and Design Foundations

Design innovations
- Region architecture (memory on pixel)
- Modular approach and distributed design
- Low current operation, fault tolerance, digital and mixed-signal test bench, etc.

Multi-site collaboration -> design repository necessary (SOS Ciosoft platform)

- Radiation hardness out of the box
- Good power distribution
  - Essential when making the long columns
- Substrate isolation (T3)
  - Essential when using standard cell synthesized logic
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Why Redesign?

• FEI4-A was submitted July 1, 2010.
  – > 30 wafers received. Evaluation and testing started in October 2010

• Can one build IBL using the FEI4-A, as is?
  Not really, because:
  - Number of design variations for test evaluations (e.g. different column flavors)
  - Calibration injection difficult
  - DAQ will be difficult- missing functions in readout architecture required to handle exceptions
  - Would need power with remote sensing on module and two voltages instead of one (same as present detector)
Fast Track IBL

• Assumptions schedule for installation 2013
  – Official FEI4-B project start: 1. March 2011
  – Construction time shortened by: explicit contingency removal (2x3mo) + parallelizing operations + early start for sensor pre-production (6-8 mo) + FEI4-B direct production run (5 mo)
  – Main construction duration of components not changed (e.g. BB, stave loading, integration …)

• The schedule is aggressive but achievable if there are no major component failures and no major delays
• There is no contingency in the schedule, which puts pressure on the designers

• Time critical items:
  – Sensor pre-production run (start Feb) and sensor review/decision (June)
  – FEI4-B submission (June 2011)
  – Bump bonding of thin modules (workplan in preparation with IZM, aim to get first thin modules in approx 3 months)
  – Stave 0 program to qualify full stave mechanically and electrically (requires rapid advancement on stave flex and module loading) (mechanical stave April-May, loaded Aug, tested Oct)
  – Beam pipe qualification of split flange and order of beam pipe
FEI4 and Module Pre-Production Schedule

<table>
<thead>
<tr>
<th>Task Name</th>
<th>Start Date</th>
<th>Finish Date</th>
<th>Duration (Work Days)</th>
<th>Predecessors</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
</tr>
</thead>
</table>

Initial FEI4-B submission plan: July
Prerequisites for the Redesign

Foremost, stay as close as possible to FE-I4A
• If it works, don't fix it.

When changes are necessary
• Try to remain backwards compatible:
  – It has to be possible to operate in “FE-I4A mode”
  – Only add the blocks that do not affect existing design
    • Prime example is the ADC/ temperature sensor block.

• Use the same version of EDA tools and flows whenever and wherever possible
• The same is true for technology libraries
• Try to stay within the existing layout boundaries to facilitate the top-level integration
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Major modifications

Complete redesign of the core part of the readout

Bias modification

Powering scheme

Added:
- Analog Mux (with buffers and filters) at the bottom of the pixel array
- ADC for remote monitoring of internal levels
- Radiation hard temperature sensor connected to ADC
- SEU immunity improvement
Pixel Array Changes

All columns in the region with pixels have now the same flavor

- Metal-to-metal capacitor used everywhere
- Changed injection switches to low-power type (to reduce leakage current to GND in off state)
- CPPM SEU latch design used in all columns
- Comparator design has also been unified
- Analog MUX (with buffers) at the bottom of the column (and chip)

![Latch Upset Map](image)
Readout Core Modification

A series of discussion and alignments with DAQ (Data Acquisition Workgroup) resulted, among others, in:

• New Data Header Format,
• Increased Bunch Counter to 13 bits, L1ID counter to 12,
• Start up improvement,
• User-programmable event size limit,
• Additional Service Records,
• ....

The highest effort, the block has been completely reshuffled
Bias Modifications

- Bandgap current reference trim bits adjusted to produce 2 uA in center of range (controlled by the bond pads and not Efuse – radiation consequence)
- 3 replicated outputs of the bandgap instead of one – additional two dedicated to shunted LDOs
- Satisfactory results concerning the temperature and process parameter gradients (0.07%/°C) per DAC spectrum

Safety-governor bit from Efuse added to the MSB of the biasing DAC – to prevent the accidental high current
A/D Convertor and Temperature Sensor

New Additions (CPPM):

- Selects one of 8 inputs to digitize, including the temperature sensor and the output of analog mux
- 10-bit output resolution
- 1.25 MHz sampling frequency

\[ T \approx \frac{q}{N \times k \times \ln M} \left( Vd_{\phi_1} - Vd_{\phi_2} \right) \]

\[ N \approx 1.00025 \]

\[ M = \frac{I_{d1}}{I_{d2}} \]
Powering Scheme

IBL distribution scheme is based on a single supply voltage

Shunted LDO modification:
- Current reference biasing
- Added startup circuit so that current reference works when power is applied
- Resistors modifications to reduce the transients

160mA of minimum current in the analog and 70mA in the digital shunted LDO
Other Modifications

• Prompt radiation detector
  – Resets the configuration, also level for firing was made higher

• Shift Register Phase Trim
  – FEI4-A bug fix

• Configuration Memory
  – Triple redundancy introduced for latch write logic; a number of configuration registers changed

• Efuse
  – Consequence of the modifications already mentioned

• Top-level interconnections and wire-bond pad ring
Design Verification Efforts

Besides the standalone block-level simulations, the following two suites for design verification have also been used:

- Open Verification Methodology Environment (OVM)
- Mixed-Signal Top-Level Testbench
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FE-I4 Evaluation

• FEI4-A testing kicked off in October 2010
  – Evaluation on wire-bonded chips
  – Functional Wafer Testing
• Testing performed mostly with USBpixTest / STctrl

The evaluation is further extended with the structural (scan-chain) test of the readout block, which makes extensive use of triple redundancy.
Yield Figures

Achieved with functional test on a number of wafers. Rather loose criteria so-far.

Yield avg. ~65%

This figure is based on functional tests only. The scan chain wafer test still needs to be carried out. Cooperation established with external test house
Scan-Chain (Structural) Test Validation
Credence Sapphire Test Flow

Sapphire uses industry standard languages including:
- XML syntax for Test Data blocks
- STIL for pattern sources
- Java for Test Templates

Go/No_Go test (structural/functional)
Scan Test Validation – Schmoo plots
Conclusion and next steps

• The FEI4-B has been taped out this month
• A sign-off review has passed
• Samples expected early November
• Production scan test will be outsourced to external test house
• The objectives of the IBL can still be met
Acknowledgement

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