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The FE-I4 Pixel Readout System-on-Chip resubmission to accommodate the Fast Track IBL plans

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The first samples of the FE-I4 engineering run (called FE-I4A) delivered promising results in terms of the merits imposed by the LHC pixel detectors. The FE-I4 team envisaged a number of modifications and fine-tuning before the actual exploitation, planned within Insertable B-Layer (IBL). As the IBL schedule was pushed significantly forward, a quick and efficient plan needed to be devised for the FE-I4 redesign. This article will present the main objectives of the resubmission, together with the major changes that were a driving factor for this redesign. In addition, design automation issues during this effort will also be addressed.

Summary 500 words

The FE-I4A integrated circuit is a first engineering run of a complex mixed-signal SoC, whose basic function is to record the time stamp and the charge of all hit pixels and transfer them off chip through the embedded readout part. The chip has been designed in 130 nm technology and contains readout circuitry for 26 880 hybrid pixels arranged in 80 columns on 250 mm pitch by 336 rows on 50 mm pitch. In general, the FE-I4 family is meant to be used with DC coupled sensors mounted on top with negative charge collection.
The preliminary measurements have been performed on a number of wafers and they revealed promising results in terms of the LHC pixel detectors performance requirements. The first actual exploitation of the FE-I4 project will take place within ATLAS Insertable B-layer (IBL). Due to the somewhat modified ATLAS shutdown timeslot, the IBL has changed its agenda, adopting and pursuing the so-called "Fast Track IBL". This had a direct consequence on the subsequent production run of the FE-I4 (called FE-I4B), meaning that the submission deadline was pushed forward to June 2011, leaving barely a few months for the redesign. Besides fixing a couple of design flaws, the major redesign effort has been mostly driven by the Data Acquisition Group (DAQ) to allow more flexibility in data stream synchronization. The DAQ requirements have been attached primarily to the End-of-Chip-Logic (EOCHL) block in the Readout part while keeping the other blocks in both region and readout part save from the redesign effort, thereby reducing the overall risks of the resubmission with tight timing schedule. The EOCHL block had to undergo several changes of which the most important ones are the programmable limit for the maximum event size, increased size of the bunch and Level1 ID counter, the modified handling of the error bit counters and the error masks in the finite state machine. The header format has also been changed inside the block. The implied modifications have been also constrained area-wise, primarily to facilitate the top-level integration with the other (not-touched) modules of the previous design. Other significant changes included the routing of the analog power supply and the introduction of general purpose ADC and temperature sensor. Also, the signal monitoring of a few internal pixel signals had to be modified. State of the art tools from the appropriate commercial EDA vendors have been used, while applying current industrial standard practices to set up and execute the design, simulation and test flow and perform the sign off. The projected date of the FE-I4B return from the second engineering run is September 2011, when a new round of characterization, including the high-volume production testing, will kick off.

Primary author: Dr ZIVKOVIC, Vladimir (NIKHEF Institute)

Co-author: Mr SCHIPPER, Jan David (NIKHEF Institute)

Presenter: Dr ZIVKOVIC, Vladimir (NIKHEF Institute)

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