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AsAd, the Front-End of the **G**eneral **E**lectronics for **T**ime Projection Chambers

... IT!

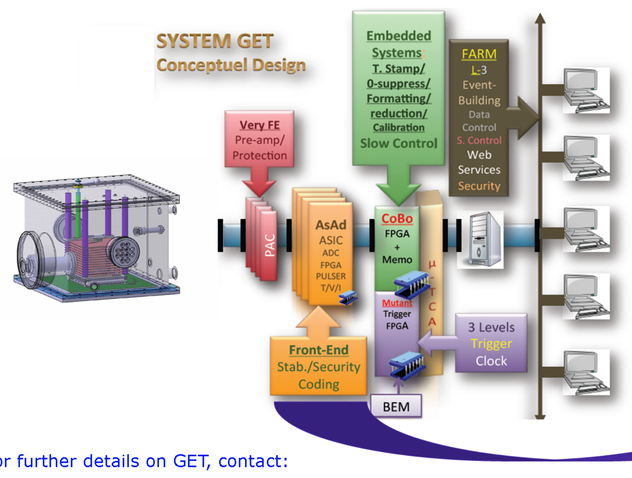
The General Electronics for Time projection chambers (GET) is a system intended to provide the nuclear and particle physicists with a complete solution to carry out experiments requiring segmented gaseous detectors. GET scope starts from the analogue signals processing to go up to the event reconstructions.

GET is developed within the framework of an international project that grew from the need of several nuclear physicists for making fine spectroscopic analysis and studying novel nuclear reaction mechanisms. For this reason, GET has been designed to be a versatile and scalable system, able to be quickly set-up and worldwide implemented.

GET Basics:

GET handles up to 30000 charge sensitive channels. Each channel stores into an analogue memory a continuously sampled preconditioned signal, while comparing its amplitude to a user-defined threshold. The number of channels over the threshold and/or any other external event triggers the sampling stop. The memory content is readout and coded, then the data is sorted (zero suppress), time-stamped, and extracted through µTCA standard, to be directed to a PC farm acting as an event builder.

GET hardware architecture is represented in **Figure 1** here-below:



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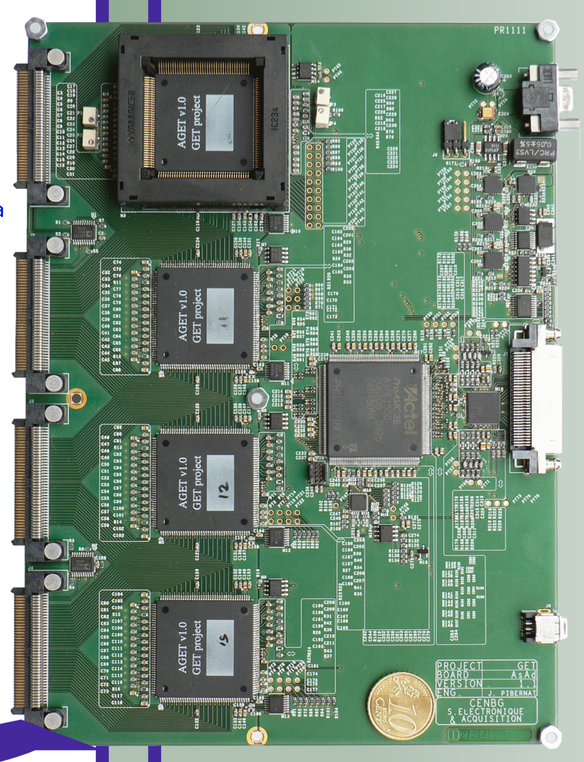
GET Collaborators

French collaborators CEA-IRFU, CENBG and GANIL financed by ANR

In the modular architecture of GET (c.f. Figure 1), AsAd is the configurable electronic board involved in the front-end signal-processing.

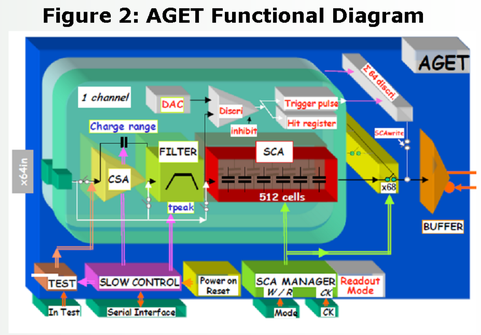
To meet its requirement, **AsAd** takes advantage of the **A**pplication **S**pecific integrated circuit designed for GET, in use together with a commercial **A**nalogue to **D**igital converter. AsAd functionalities have been implemented around these 2 main parts which major features are firstly overviewed.

AsAd supports **4 AGET** (**A**SIC for **GET**) each one composed of **64 channels** dealing with as many detector-pads signals. As shown in Figure 2, one channel includes:



- A Charge Sensitive Amplifier (**CSA**) operating on one charge range selectable among 4 available (±120fC, ±240fC, ±1pC and ±10pC)
- An analogue filter (**shaper**) with a selectable peaking time value (16 available values from 70ns to 1µs)
- An output-width adjustable **threshold-discriminator** associated to one memory-cell tagging the threshold crossings (The 64 cells concatenation is called "hit register")
- A 4-bit Digital to Analogue Converter (DAC) for trimming the channel threshold given by another 4-bit DAC common to all channels
- A splittable **512-cell analogue circular memory** based on a Switched Capacitors Array (1x512 cells memory depth can be changed in 1x128 cells, 1x256 cells or 2x256 cells according to the user requirements)

Figure 2: AGET Functional Diagram



AGET standard operation consists in continuously sample the 64 shapers outgoing signals while comparing their amplitude to the global threshold. At the same time, the discriminators output signals are summed and the result is extracted from AGET trough its output buffer. This signal is coded by AsAd's ADC and when the coded sum reaches a given value (multiplicity threshold), the sampling is stopped. Then the analogue memories contents have to be readout. This operation can be achieved within 1 of these 3 available modes : "All channels", "Hit channels" (crossed threshold) and "user-defined channels". During this process the analogue samples are cell-by-cell extracted trough the AGET output buffer and on-flight coded by AsAd's ADC.

A quad-channel, **12-bit ADC with serial LVDS interface** is implemented onto AsAd (Each channel input connects an AGET output). One ADC data is serialized and output over two LVDS pairs (2-wire interface, 6 bits on each pair). In this configuration, the AsAd data rate transmission rises up to **1.2Gbit/s**. This transmission is synchronized by two clocks synthesized from the ADCs sampling clock, by an on-chip Phase Lock Loop (PLL).

The **ADC** sampling **clock** derives from an AsAd external reference clock at **25MHz**. This reference is processed by a **FPGA** clock conditioning circuit able to phase-shift the AGET readout clock from the ADC sampling clock, and to keep them synchronized.

Another PLL-based clock conditioning circuit is also used to control the **AGET sampling clock** phase. This clock's frequency is externally set **from 1MHz to 100MHz** (depending on the detector drift-time) but its phase can be locally adjusted to keep all AGET synchronized in a complete system (**128 AGET, 200ps resolution**)

All the above configuration parameters are settable by slow control trough **5 serial ports** (1 per AGET and 1 dedicated to all the other AsAd devices). **3-wire interfaces** supporting a **SPI** based **protocol** have been implemented in order to keep as low as possible the number of connections at the AsAd/Command-Control interface. The ASICs protocol decoders operate at 25MHz and the board protocol decoder operates at 10Mhz.

As shown in Figure 3, this one is not only used to set the ADC and the FPGA clock conditioning circuits configuration, but also to control these implemented utilities:

- A Test & Calibration manager allowing the calibration of AGET channels through an AsAd **embedded pulse generator**
- A **monitor** able to protect AsAd from failure by continuously checking its supplied **voltage** and **current** as well as its **temperature**
- A **digital inspection** manager able to output AsAd's main signals for diagnosis
- An **identifier** allowing to track the AsAd position in the whole GET system as well as to find its serial number
- An input manager able to switch voltages out of AsAd in order to disconnect some detector dead areas as well as to bias external protection circuits to prevent AGET inputs from detectors sparks

The figure 4 here below shows the time sequence for testing AGET SCA splitting.

"SCA write" signal enables the AGET sampling clock. Then AsAd embedded pulser is triggered. The voltage pulse is applied to an AGET internal capacitor in order to stimulate the CSAs input. For each channel, the signal is conditioned, sampled and stored into the first half of the switched capacitors array until the sampling clock inhibition. Then, the same sequence is repeated but the signal is sampled and stored in the second half of the switched capacitors array. At the end of the sampling the first and second halves of the memory are consecutively readout.

Using this operational mode, the **dead-time** between two consecutive events (e.g. implantation/decay) can be lowered down to **30ns** with a 100MHz sampling clock

Figure 4: Splitted SCA Readout

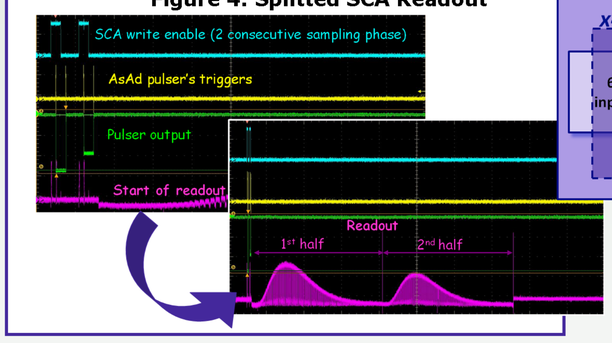
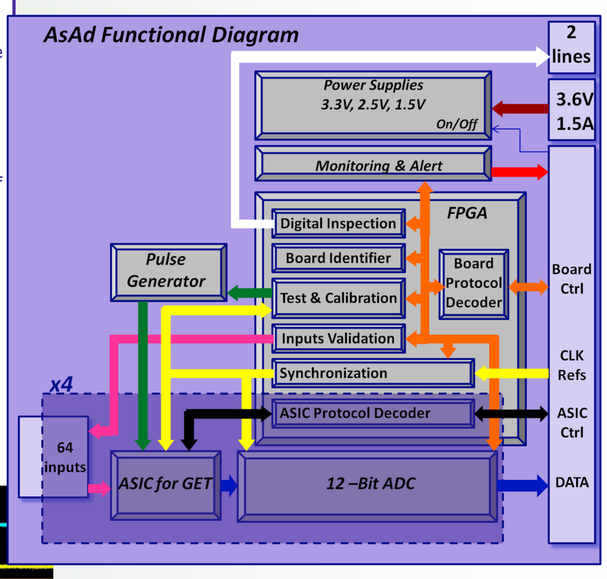


Figure 3: AsAd Functional Diagram



An AsAd prototype (dimensions 210mm x 154mm) has been produced. The power consumption of the full loaded board is lower than **5W** on a **3.6V** supply voltage. All AsAd functions have been successfully tested with **3m-distant** command -control and DAQ systems.

The GET front-end characterization is currently running. AGET is firstly under characterization and the AsAd prototype is used as a test bench. The full AGET characterization is expected at early 2012.

A GET demonstrator is expected at the end of 2013. For this demonstrator an AsAd version enclosed in a 12mm-thick shielded shell will be proposed. This shell will also water-cool AsAd in order to keep it as close of the detector as possible.

Desired performances for GET: reaching a 60dB SNR (full-scale signal) at 1kHz event rate, with 10% occupancy of a 30 000-channel detector.