

# KLauS - A Charge Readout and Fast Discrimination Chip for Silicon Photomultipliers (SiPMs)

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KLauS is an ASIC in AMS 350nm Bicomos Technology with 12 Silicon Photomultiplier (SiPM) readout channels. It is designed to be used in the plastic scintillator based Analog Hadron Calorimeter (AHCAL) at a future Linear Collider. Its dynamic range reaches 200pC and SNR is better than 10 for single photon signal of very low gain SiPMs. The chip provides 2V bias tuning to compensate SiPM breakdown voltage variations. The measured timing jitter is 50ps for nominal AHCAL MIP response (15 pixels fired). Power pulsing option has been implemented such that one can make use of ILC bunch crossing clock structure. The total power is 25uW.

## Summary 500 words

KLauS chip is designed to be used in the ILC organic scintillator-based analog hadronic calorimeter with SiPM readout. One of the main constraints for such a calorimeter is a very dense structure leaving minimal space for infrastructure and readout. As a consequence one of the major requirements for the front-end electronics is a very low power consumption to avoid active cooling; a value of 25 uW per channel is achieved with the chip without affecting any of the built-in readout capabilities. A power pulsing scheme utilizing the ILC bunch pattern (198 ms gap after 2 ms of collisions) has thus been implemented to achieve low system power consumption. The chip functions as follows. The detector signal totally flows into the chip due to its low input impedance at the input stage. The current is integrated on a passive integration unit and dc coupled into later processing stage. The shaper is an active filter, which adds two complex poles to the integration pulse so as to provide an output waveform without any undershoot. A 6 bit microwatt DAC controls the voltage on the input signal line and therefore used to finely tune the sensor bias voltage with a total range of 2V. A multi-gain selection unit can be designed to process the signal with different amplification. The signal can be scaled down by factor 1, 10 or 40. The total dynamic range has been measured to be more than 200pC of the lowest gain settings with an integral non-linearity of 1%. The input-referred ENC is measured to be 25000 e- with detector capacitance of 40pF, which makes the SNR better than 10 even for very low gain SiPMs. The shaping unit provides a shaping selection of 25 ns, 50 ns and 100 ns. Due to the fast recovery time, the channel is also capable of handling dark noise of several MHz. Very nice single photon spectrum has been measured with the chip even using very low gain SiPM ( $2.75 \cdot 10^5$ ) and high dark count rate ( $\sim 1$  MHz). For every input signal, a trigger can be generated according to different threshold values and it can even be set well below single pixel signal. Hence, single photon triggering is also possible with the chip. The measured timing jitter is 50ps for a charge injection of 600fC through 33pF capacitance which corresponds to a nominal MIP response of AHCAL with 15 pixels fired using very low gain SiPMs. In addition, all the channels are able to provide a stable dc input voltage at all times despite the power pulsing clock scheme at all preset DAC values. This chip feature stems from the special feedback scheme at the input stage. The voltage difference between clock "on" and "off" stages is less than 20mV, which only corresponds to 1-2% of the SiPM bias voltage and is certainly negligible. This voltage can be decreased down to 5mV with an off-chip resistance. The recovery time is only tens of micro-seconds. The total power is less than 2mW per channel and decreases to 25uW with ILC power scheme.

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