Evaluation of Emerging Parallel Optical Link Technology for High Energy Physics

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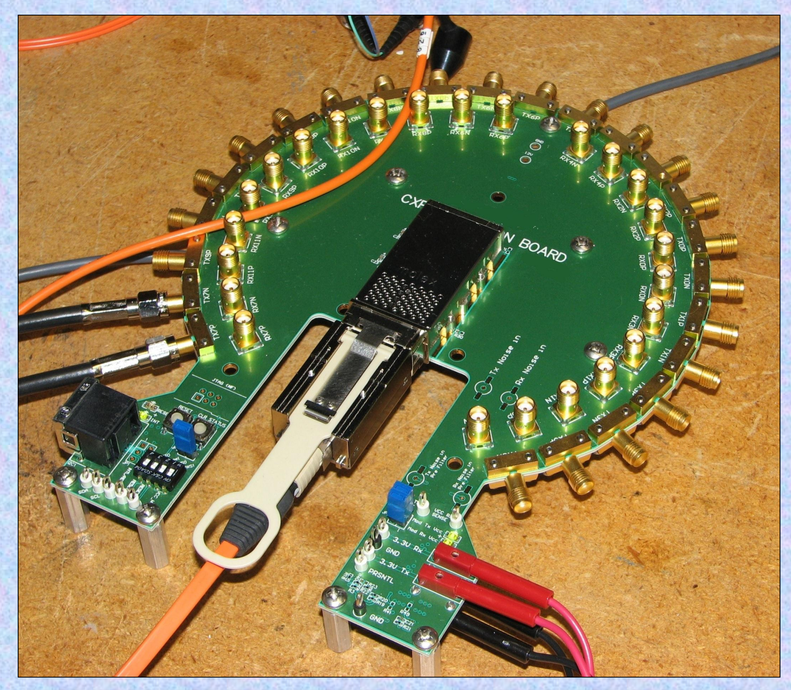
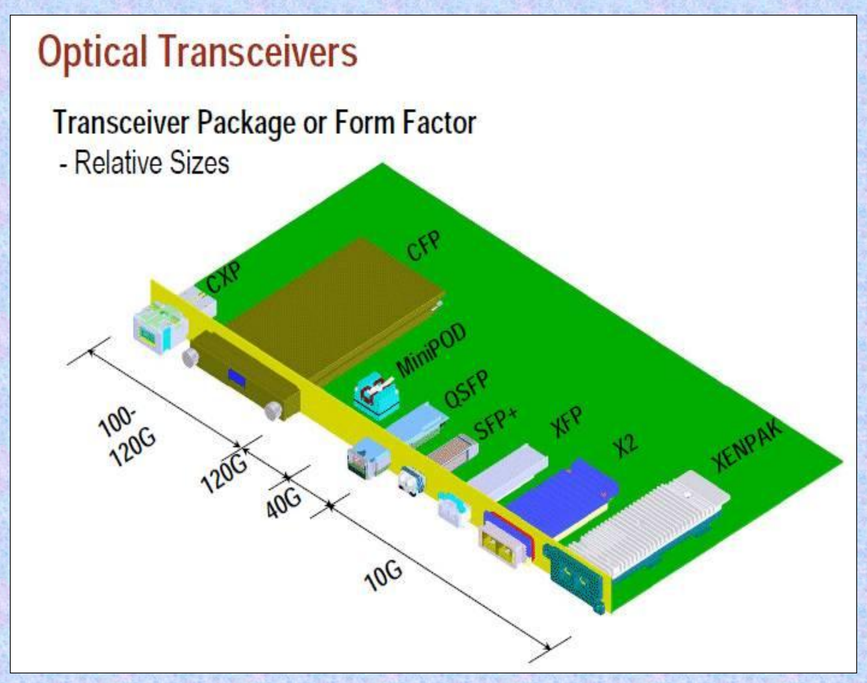
Abstract

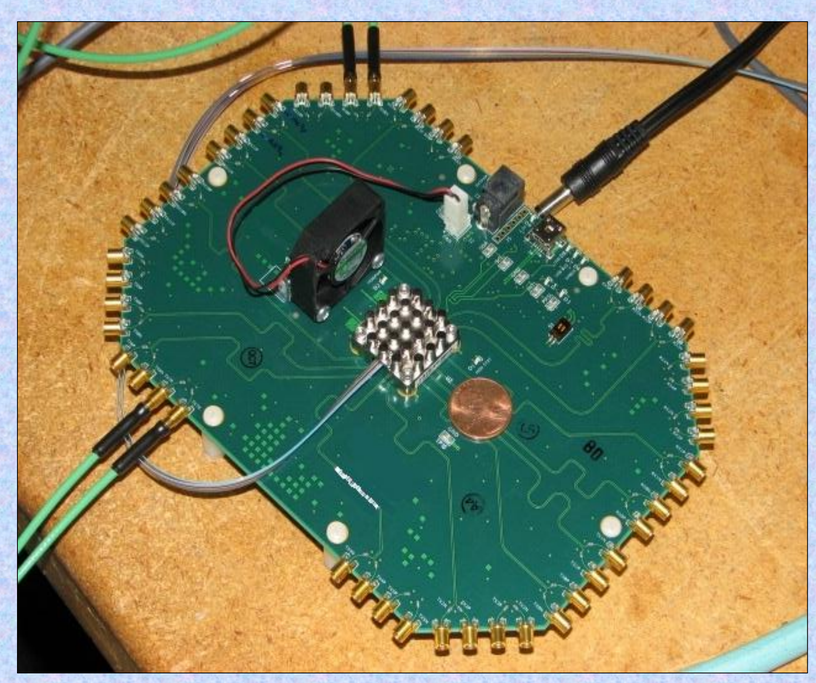
Modern particle detectors utilize optical fiber links to deliver event data to upstream trigger and data processing systems. Future detector systems can benefit from the development of dense arrangements of high speed optical links emerging from industry advancements in transceiver technology. Supporting data transfers of up to 120 Gbps in each direction, optical engines permit assembly of the optical transceivers in close proximity to ASICs and FPGAs. Test results of some of these parallel components will be presented including the development of pluggable FPGA Mezzanine Cards equipped with optical engines to provide to collaborators on the Versatile Link Common Project for the HI-LHC at CERN.



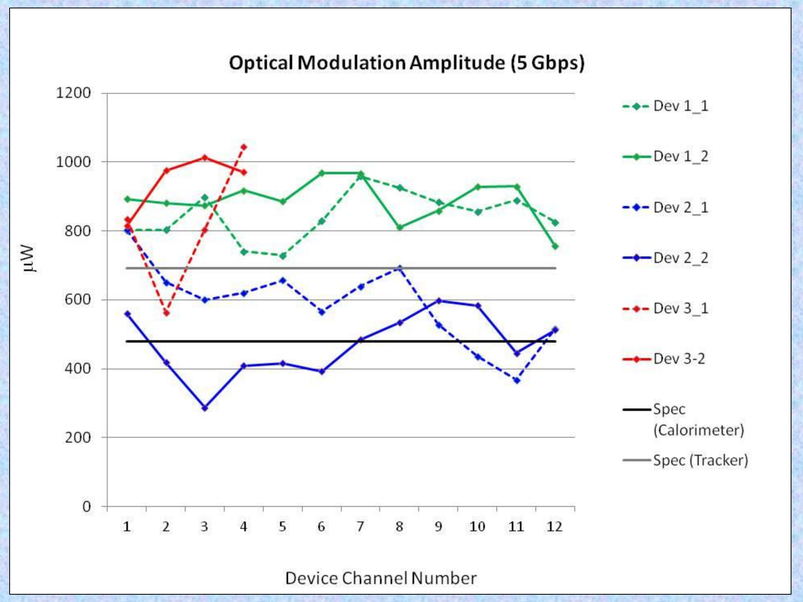
The figure above illustrates a 12 channel parallel transceiver designed for 120 Gbps operation in each direction. This device is mounted on an evaluation platform for convenient characterization of the electrical and optical performance of the module. A 24 fibre ribbon is attached to the module which is inserted into a metallic carrier. SMA connectors around the board are used to convey transmit and receive electrical signals which interface to an FPGA signal integrity kit (not shown) for bit error rate tests.



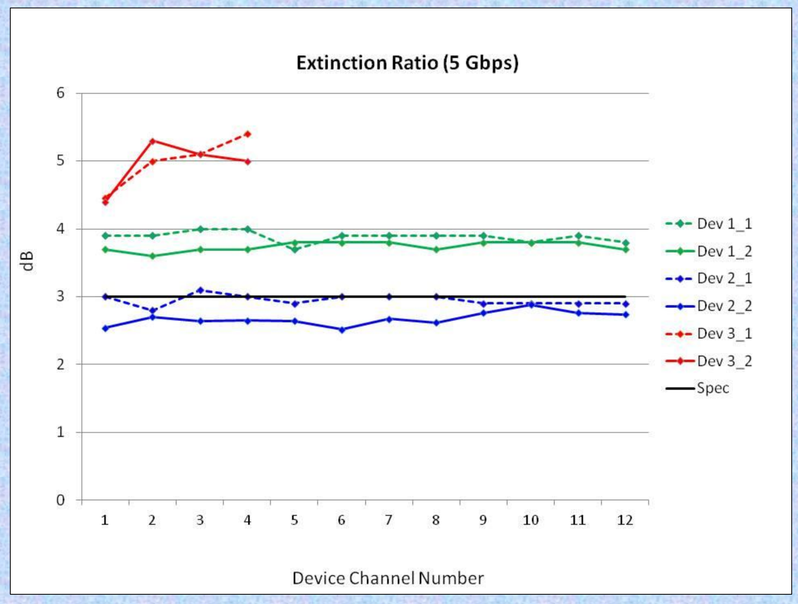
This figure illustrates the trend in optical communications components towards higher channel speeds and greater parallelism. The SFP+ component in the center of the figure is the single channel standard adopted for back end components of the Versatile Link Common Project. Emerging parallel devices are becoming available which match the 10 Gbps channel rate of the SFP+ standard in 4 and 12 channel products. An example is the MiniPod Optical Engine. (Image courtesy of Avago Technologies)



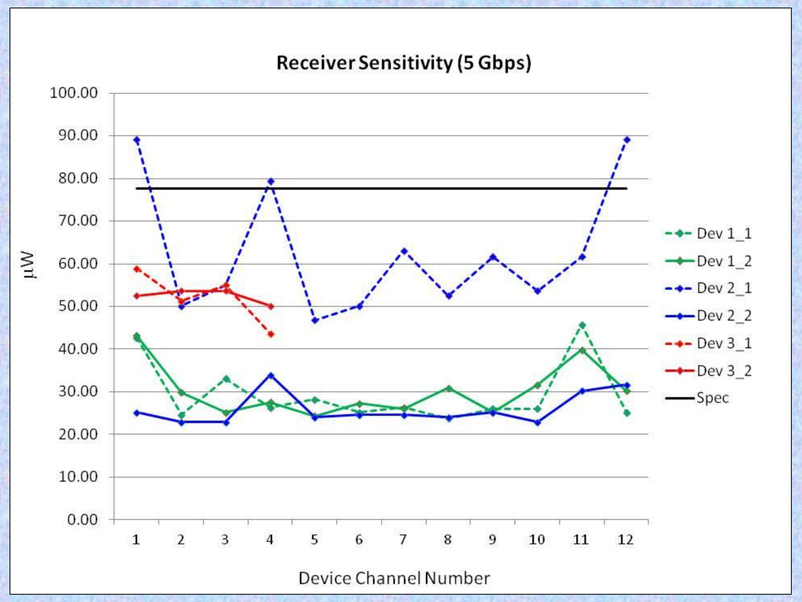
This figure illustrates a second 12 channel parallel transceiver designed 120 Gbps in each direction. This device is mounted mid-board with a heat sink and a 24 fibre ribbon pigtail. The mid-board mounting of the optical engine transceiver allows printed circuit board designers greater flexibility in the layout and routing of boards utilizing the technology. The optical engine is secured to the evaluation platform with screws and the electrical contacts with the board are made with an array of spring contacts mating with pads.



Measurements of Optical Modulation Amplitude (OMA) as a function of channel number for two 12 channel transceivers (Dev 1 and Dev 2) and a 4 channel transceiver (Dev 3). Two components of each of the device types were tested. All devices were operated at 5 Gbps to demonstrate performance at the operating data rate of the Versatile Link. These results indicate performance compared with the Versatile Link parallel channel threshold for calorimeter grade and tracker grade links.

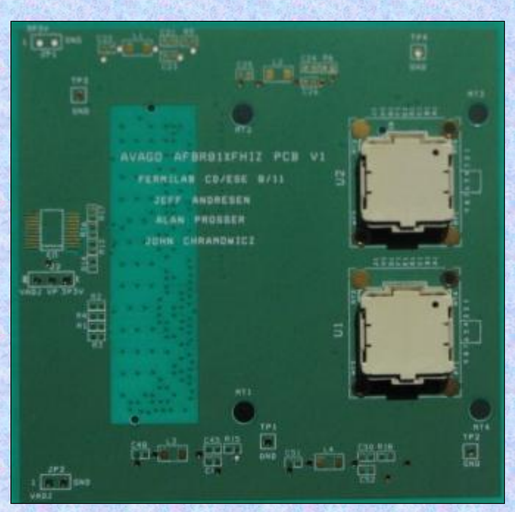


Measurements of Extinction Ratio (ER) as a function of channel number for two 12 channel transceivers (Dev 1 and Dev 2) and a 4 channel transceiver (Dev 3) at 5 Gbps. These results indicate that not all of the devices are able to meet the performance requirements for the Versatile Link. One type of device (Dev 2_1 and Dev 2_2) fails to meet the threshold while the other two devices performance adequately to pass the requirements of the Versatile Link per channel specification.



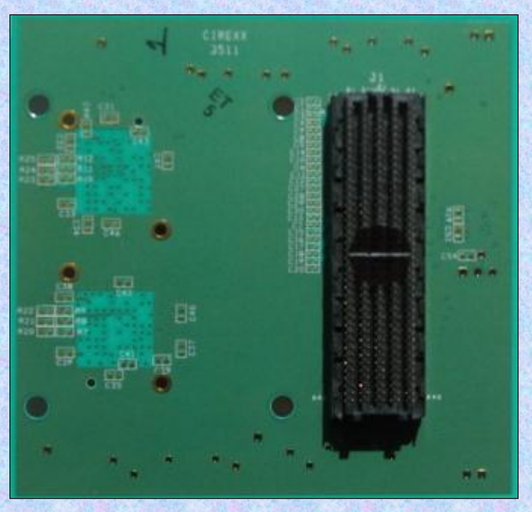
Measurements of Receiver Sensitivity as a function of channel number for two 12 channel transceivers (Dev 1 and Dev 2) and a 4 channel transceiver (Dev 3) at 5 Gbps. Two components of each of the device types were tested. These results indicate that one device tested (Dev 2_1) failed to meet the per channel specifications of the Versatile Link. One other example of that same device family (Dev 2_2) however did meet the performance requirements. As these devices are emerging products, additional testing is warranted.

The image at right shows two Meg Array sockets which will host a 12 channel transmitter and a 12 channel receiver on an FMC equipped mezzanine card. This card, developed by Fermilab, will be available to Versatile Link collaborators for testing with parallel optics



Future Work:

Fermilab will continue to characterize promising devices to determine the most suitable components available for use in Versatile Link compatible systems. These tests will be expanded to include reliability and environmental tests. In addition, FMC-based test cards will be developed for any new parallel optics transmitters, receivers, and transceivers as they emerge and will be made available to collaborators. The results of these tests will lead to a suite of recommended back end array components for the Versatile Link Common Project. The possible application of array technology is also being pursued for front end detector opto-electronics as well.



The image at left shows the FMC connector on the bottom side of the same test card which will host a 12 channel transmitter and a 12 channel receiver. High speed electrical signals are conveyed to and from suitable FPGA based test platforms over this connector.

Summary:

As part of the Versatile Link Common Project, Fermilab is continuing the evaluation of several options in commercially available and prototype parallel optical communications products. Specifications which state the performance requirements for each transmitter and receiver channel of parallel devices have been produced and are used as the criteria by which the performance of promising devices are judged. In addition to testing these devices, Fermilab will continue to work with vendors to pursue improvements to device performance, packaging, and their use in Versatile Link systems.

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