Contribution ID: **126** Type: **Poster**

Design of a ”Digital Atlas Vme Electronics” (DAVE) Module

Thursday 29 September 2011 16:00 (2h 30m)

ATLAS-SCT has developed a new ATLAS trigger card, ‘Digital Atlas Vme Electronics’ (”DAVE”). The unit was designed to provide a versatile array of interface and logic resources, including a large FPGA. It interfaces to both VME bus and USB hosts.
DAVE aims to provide exact ATLAS CTP functionality, with random trigger, simple and complex deadtime, ECR, BCR etc. being generated to give exactly the same conditions in standalone running as experienced in combined runs.
DAVE provides additional hardware and a large amount of free firmware resource to allow users to add or change functionality.

Summary 500 words

ATLAS-SCT has developed a new ATLAS trigger card, ‘Digital Atlas Vme Electronics’ (“DAVE”). The unit was designed to provide a versatile array of interface and logic resources, including a large FPGA. It interfaces to both VME bus and USB hosts.

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DAVE communication is by standard VME or by USB, allowing use inside VME-TTC crate or stand-alone on a bench-top. For this reason, +5V is the single power input (from the VME backplane or a stand-alone power supply), with all other power buses being generated on-board.

Firmware is developed in a modular fashion allowing code contributions from interested users. Initially the core SCT requirements (vetoing trigger generation around a BCR) will be implemented.

Further development will aim to provide other CTP functionality, with random trigger generator up to 100kHz, simple and complex deadtime, busy gating, ECR, BCR, etc. generation to give exact same conditions in standalone as experienced in combined runs.

Firmware for this purpose is being copied from the CTP code to ensure identical operation.

Some other useful capabilities include BC/ORBIT source with fine-delay (with 0.5nsec resolution) for timing scans, generic counter facility, etc.

In addition, a large ‘trigger sequence record / playback’ is incorporated on a 72Mbit SRAM. This provides up to 52 seconds history of trigger playback at 75 kHz L1 trigger rate (e.g. on interrupt by system BUSY).

The final design is a single 6U VME card with 2 clock inputs and outputs (as NIM or ECL on LEMO connectors) and 8 programmable data inputs and outputs (as NIM or TTL on LEMOs), containing a large Xilinx Spartan 3E 1600 (XC3S1600E-FCG400C) FPGA, 4Mbx18 SRAM (GS8642Z18GB 1671), on-board 80.15733MHz clock X-tal generator, PLL (ICS581-02) and CERN ‘Delay25’ delay lines, together with a 40-pin expansion header for possible daughter card(s).

Total of three prototype DAVE modules have been produced and tested by Cambridge and UCL. Further 17 production modules are being manufactured, with some modifications based on the test results, to be delivered to users in the autumn 2011. Additional firmware, suggested by various potential users, is also being developed.

The hardware design is described, together with various test results of the three prototype boards tested.

Description of available firmware is also included, together with some interesting use-cases examples.

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Session Classification: Posters

Track Classification: Systems