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Developments at the UC Davis Facility for Interconnect Technologies

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As silicon detectors in HEP require increasingly complex assembly procedures, the availability of a wide variety of interconnect technologies provides more options for overcoming obstacles in generic R&D. I present recent progress and challenges faced in various interconnect technologies: gold stud and double gold stud bonding, deposition and bonding of indium bumps, solder ball bonding and dispensing and bonding using conductive epoxy. Advantages and limitations of each technique are analyzed to provide insight into potential applications for each method. Optimization of procedures and ideal parameters for each technique, developed at the UC Davis Facility for Interconnect Technology, are presented.

Summary 500 words

As HEP moves towards higher center of mass energies and luminosities, silicon detectors require increasingly dense assemblies and hence more sophisticated interconnect techniques to handle new challenges. The UC Davis Facility for Interconnect Technologies (UCD-FIT) is developing various technologies to solve a wide variety of problems and to provide support for researchers involved in generic R&D.

Gold stud bonding is a well-understood method of providing a strong metallurgic connection between two metal surfaces and forming a highly conductive bond without the need for complicated photolithography. This is important for die-level bump bonding. A high voltage arc is used to form a small sphere at the end of a thin (approx 1 mil) Au wire, which is then lowered onto the bonding pad and a stud is formed by ultra-sonication. The studded chip is then bonded to another device through thermo-compression. We have determined the parameters that provide low-resistance bonds with high mechanical strength, yield and repeatability. This process is limited by the threshold of pressure the material can handle and the need to have gold surfaces on the opposing chip.

The need for gold surfaces is eliminated by the use of double gold studding. In this procedure, gold studs are formed on typical aluminum pads of both of the chips to be bonded, and their top surfaces are flattened by "coining". During flip-chip bonding, this has the added advantages of requiring less pressure to achieve strong adhesion compared to single bumps, and a taller connection should the packaging require it. I will present the ranges of pressures and temperatures at which the process provides the greatest conductivity.

Indium bumps provide an option for connecting smaller pads down to 10 um. Photolithography followed by chemical vapor deposition is used to form indium bumps of desired height. The use of a photomask allows us to form a large number of small bumps and process multiple wafers simultaneously. UCD-FIT has also developed a unique method for photolithography on a single die by using polydimethylsiloxane (PDMS) to embed the chip, thus eliminating any edge beading during the spinning of photo-resist. Cold-welding of indium also allows for a greater number of bonds to be made with less pressure required, reducing risk of damage to delicate devices.

Conductive epoxy is a versatile material that can be used stand-alone or in conjunction with other interconnect techniques, such as gold studs. It can provide strong mechanical and electrical connections by itself, while reducing the amount of pressure when used with gold studs, thus lowering the risk of damaging devices. Epoxy dispensing on a large number of pads can be automated through the use of numerically controlled robotic arm available at UCD-FIT.

I will present results on technologies discussed above: development of solder-ball bonding and anisotropic conducting films for the Si-W calorimeter project will be presented in a talk submitted by Michael Woods to TWEPP. I will also discuss progress made for a CMS track-trigger prototype and bump-bonding support provided to the Large Area Picosecond Photodetector project.

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