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Characterisation Of The NA62 GigaTracker End of Column Demonstrator Hybrid Pixel Detector

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The architecture and characterisation of the NA62 GigaTracker End of Column Demonstrator Hybrid Pixel Detector (HPD) will be presented.
This detector must perform time stamping to 200 ps (RMS) or better,
provide 300 μm pitch position information and operate with a dead time of 1 % or less for 800 MHz–1 GHz beam rate. The demonstrator HPD Assembly comprises a readout chip with a test column of 45 pixels, alongside other test structures, bump bonded to a p-in-n detector 200 μm in thickness. Validation of the performance of the HPD and the time-over-threshold timewalk compensation mechanism with both beam particles and a high precision laser system was performed. Confirmation of better than the required time stamping precision has been demonstrated and will be shown alongside other pertinent results.

Summary 500 words

The NA62 GigaTracker (GTK) hybrid pixel detector comprises three stations situated early in the beam line, designed to measure the momentum, angle and traversal time of the beam particles. The requirements on these parameters are driven by the demanding background rejection level necessary for the rare kaon decay measurement. In total, the beam rate incident on the GigaTracker is expected to be around 800 MHz – 1 GHz, which equates to approximately 140 kHz per pixel in the centre, where the intensity is the highest. The total dead time of the detector is required to be less than 1%. The radiation environment is expected to be extremely harsh, with the total dose per year approximately 10ˆ14 1 M eV n eq.: similar to that expected in 10 years of operation for a central tracking detector in an LHC experiment.

Each detector instruments an area of 60 mm x 27 mm and consists of an array of 18000 pixels, each one nominally 300 x 300 μm2 . Time stamping is required to the level of 150 ps (RMS) for the GigaTracker as a whole and better than 200 ps (RMS) per station. A demonstrator readout ASIC and detector were designed and fabricated and have undergone extensive combined and independent electrical, laser and beam testing. Architecturally, this design is based on an asynchronously operating pixel matrix with a single threshold discriminator per pixel. Hit time stamping is done in the end of column region by a delay locked loop based time-to-digital converter. A time over threshold measurement, coupled with an off-detector look-up is used to effect the discriminator time walk correction. Discrepancies between the time resolution measured with particles during the beam test and that measured in the lab with the laser system were significant and warranted investigation. A detailed study of the behaviour of the sensor and readout electronics was subsequently undertaken to identify and characterise these additional contributions to the timing resolution seen with particles. The demostrator system exhibits a time-stamping resolution of better than 200 ps (RMS) per station for single particles.

A significant effort is underway at present to design the readout ASIC required for the final system, now dubbed TDCPix. This chip will instrument a tenth of the total area per station with 40 columns of 45 pixels. A description of this ongoing work will be included.

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