**The Front-End Concentrator card for the RD51 Scalable Readout System**

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**THE SCALABLE READOUT SYSTEM (SRS)**

Mandated to establish a "Portable Multichannel Readout system for Multi Pattern Gas Detectors", the Scalable Readout System (SRS) was developed within the RD51 collaboration as a complete readout system for gas detectors like GEMs or MicroMegas, and not excluding other types of detectors.

Goal: to provides a choice of ASICs, hybrids or discrete frontends, with analog or digital readout, which are connected to the SRS readout via a common interface.

Programmable trigger and large event buffer allow different trigger and buffering schemes

Large systems (>16 channels) require the Scalable Readout Unit (SRU) for aggregating up to 40 FECs to 10 Gb/s Ethernet network ports of an Online PC or farm. For small systems, the FECs are directly connected via Gigabit Ethernet cables to the Online Computer running ALICE's DATE software.

**ADAPTER CARDS AND MECHANICS**

Three different FEC adapter sizes (A, B and C) are defined, with design rules freely available to the SRS developer community.

The ensemble (FEC/adapter, edge mounted) forms a 4x4 220 mm Eurocard that fits on a 19" subchassis

- Can be used as generic 16 ch 12-bit 50 MHz ADC
- Interface to the RD51 APV25 ASIC hybrid
- Interface to the RD51 Beetle ASIC hybrid
- PMT readout in the NEXT experiment
- Interface to digital front ends
- Clock and trigger interface & distribution
- In NEXT, used to interface the SPM readout

**Features:**

- Xilinx Virtex-5 LX50T FPGA
- On board 256 Mbyte DDR2 event buffer
- 3 multi-gigabit transceivers to A, B, conn.

**A- Connector:**

72 I/Os configurable as single-ended or differential with selectable signaling levels

**B- Connector:**

16 I/Os configurable as single-ended or differential with selectable signaling levels

The module is currently being upgraded in order to incorporate a four times larger and faster data buffer (DDR3 6GB), increased processing power (larger Virtex-6 FPGA), enhanced SEU and EMI immunity, compatibility with high B-field environments and an additional SPF+ slot to increase the module throughput and/or to allow Ethernet-based slow controls.

**WANT TO DEVELOP A NEW READOUT APPLICATION?**

Contact RD51 WG1 Converters (Hans Muller at CERN PH-AID and Jochen Kaminsky at Bonn University)

RD51 aims at providing its users:

- Adapter card design specifications (in case the existing adapters do not suit your application)
- FPGA firmware for basic blocks (FI0-like Interfaces to GbE Ethernet and DDR2, slow controls Interface)
- ALICE's DATE online system is provided by CERN-PH under agreement
- Production and development cost reduction due to a growing base of users and developers
- Access to future applications

You will provide:

- Data path firmware (i.e., your application-dependent data processing)
- I/O firmware (in case you develop a new adapter card)

The FEC card is currently being used or evaluated in several applications like:

- Readout of PMT and SPM sensors in the NEXT Collaboration
- Muon tomography for detection of high-Z materials in cargo ( homeland security), Florida Institute of Technology
- NA62, MicroMeGas-based reference tracker station
- UNAM Mexico, THGEM readout station
- Characterization of GEM foils at the Helsinki Institute of Physics
- Readout of resistive strip MM as upgrade to ATLAS detector
- Muon tomography for water quality control in South of France
- GEM Chamber project (Lyon Lab) and GEM readout via SRS (BNL)

Future applications also include BEETLE, VPAT ASICs and future CERN GBT front-end readout

**REFERENCES**

3. See: http://indico.cern.ch/sessionDisplay.py?sessionId=19&contribId=46&confId=132080

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