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The Front-End Concentrator card for the RD51 Scalable Readout System

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The Scalable Readout System (SRS) was developed within RD51 collaboration as a multi-channel readout system, allowing ASICs, hybrids or discrete frontends with analog, binary or digital readout over a customizable link interface. User-specific frontends are linked to adapter cards which are straddle-mounted to Front-end Concentrator cards (FEC). The ensemble (Adapter + FEC card) forms a 6Ux220 mm unit.

The most common adapter card is a 16-channel ADC card for analogue frontends like the APV25 or Beetle-based hybrids. More adapter cards for digital or more specific applications are existing or under design.

Dozens of other applications are starting and a fast growing community of users and developers is working on SRS hardware, firmware and software.

Summary 500 words

The Scalable Readout System [xx] was developed within RD51 collaboration as a multi-channel readout system, allowing to choose ASICs, hybrids or discrete frontends with analog, binary or digital readout over a customizable link interface to the standard SRS readout electronics. A small system consists of a user-specific frontend that is linked to frontend adapter cards which are straddle-mounted to Front-end Concentrator cards (FEC). The FEC is an FPGA-based data concentrator which connect the SRS electronics via Gigabit Ethernet to an Online system. A minimal SRS system consists of a single Adapter + FEC card, forming a 6U x 220 mm unit. Stacked in a 19"subchassis, 8 Adapter/FEC units can readout up to 16k channels. Up to 5 subchassis can be star- connected to a Scalable Readout Unit (SRU) which forms SRS readout clusters up to 96 k channels. Larger SRS systems consist of several SRU clusters.

The most common SRS adapter card is a 16-channel, 12-bit ADC card for analogue frontends like the APV25 or Beetle-based SRS hybrids. More SRS adapter cards for digital or more specific applications are under design.

Conceived as a RD51 partnership project between CERN and Universidad Politécnica de Valencia, the FEC card was designed as a general-purpose SRS data concentrator with generic interface for SRS adapter cards. The FEC output link is Gigabit Ethernet towards the default DATE Online system of SRS. First small and medium-sized SRS systems are in use: PMT and SiPM sensor readout for the NEXT experiment, Muon tomography with GEMs at the Florida Institute of Technology, characterization of GEM foils at the Helsinki Institute of Physics and upgrade of the ATLAS CSC readout with resistive-strip Micromegas. Dozens of other SRS applications are starting and a fast growing community of SRS users and developers is working on SRS hardware, firmware and software.

The FEC card is designed around a Xilinx Virtex-5 FPGA and a 256-Mbyte DDR2 buffer. I/Oconnectivity include a SFP module for gigabit Ethernet (interface to the online system), NIM and LVDS I/O, two RJ-45 sockets (4 LVDS pairs each) and more than 100 configurable lines between the FPGA and the adapter card.

The module is currently being upgraded in order to incorporate a four times larger and faster data buffer (DDR3 SODIMM), increased processing power (larger FPGA), enhanced SEU and EMI immunity and three additional SFP+ slots to increase the module throughput and to allow Ethernet-based slow controls.

This presentation will show the design and applications of the FEC card in the context of the RD51 Collaboration.

Comments:
* See WG5 session at https://indico.cern.ch/conferenceTimeTable.py?confId=132080#20110414 for more detailed information on the current applications and plans for the FEC module.

- See https://espace.cern.ch/rd51-wg5/Shared%20Documents/SRS-Short-description-1.pdf for an introduction to SRS.

[xx] "The Scalable Readout System (SRS) for Micro Pattern Gas Detectors and other Applications"H. Muller et al. to appear in NIM

Authors: Dr MULLER, Hans (CERN); Dr TOLEDO ALARCÓN, José Francisco (Valencia Polytechnic University)

Co-authors: Mr TARAZONA MARTÍNEZ, Alfonso (Valencia Polytechnic University); Mr CATALÁ PÉREZ, Joan Marc (Valencia Polytechnic University); Mr MONZÓ FERRER, José María (Valencia Polytechnic University); Dr ESTEVE BOSCH, Raul (Valencia Polytechnic University); Mr MARTOIU, Sorin (CERN)

Presenters: Dr MULLER, Hans (CERN); Dr TOLEDO ALARCÓN, José Francisco (Valencia Polytechnic University)

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