Contribution ID: **55** Type: **Poster**

A multichannel Time-to-Digital Converter (TDC) inside a Virtex-5 FPGA on the GANDALF module

Thursday 29 September 2011 16:00 (2h 30m)

The GANDALF 6U-VME64x/VXS module has been developed for the digitization and real time analysis of detector signals. Based on this platform, we present a 128-channel TDC which is implemented in a single Xilinx Virtex-5 FPGA using a shifted-clock-sampling method. A particular challenge of this algorithm is the predictable placement of the logic components and the uniform routing inside the FPGA. We present measurement results for the time resolution, the differential nonlinearity and the rate capability of the TDC readout system.
This project is supported by BMBF and EU FP7.

Summary 500 words

The GANDALF 6U-VME64x/VXS module has been designed to cope with a variety of readout tasks in high energy and nuclear physics experiments. Therefore this module comes with exchangeable analog and digital mezzanine cards to perform different applications such as analog-to-digital or time-to-digital conversions, coincidence matrix formation, fast pattern recognition and trigger generation.

GANDALF equipped with digital input mezzanine cards allows to connect up to 128 LVDS signals in parallel and thus the employment of the system as a multichannel TDC. The time-to-digital conversion is done by a Virtex-5 FPGA on the mainboard using a shifted-clock-sampling method.

In this TDC concept, each input signal is continuously sampled by eight flip-flops with equidistant phase-shifted clocks. As a result, this algorithm demands for keeping the skew of the data signal routing to a minimum. Therefore predictable placement of the logic components and uniform routing inside the FPGA fabric is a particular challenge of the design. Furthermore the output of all sampling flip-flops is not stable at the same time due to the different clock domains. For this reason, partitioning of the output bit pattern for hit selection is necessary using this method. With currently 388.80 MHz sampling clock frequency, less than 100 ps time resolution of the TDC can be achieved.

The measured time information is stored in Hit Buffer RAMs for each channel inside the FPGA. Whenever a trigger signal is received by the GANDALF module, a time stamp for the trigger is generated. A forward or backward looking 'Trigger Matching Unit', which is included inside the FPGA logic, checks the stored data time stamps for correlations in time to the experiment trigger. This allows to pass only hits within a variable time window around a given trigger signal to the output bus and thus to reduce the overall data transfer rate.

As there are also digital output mezzanine cards, the GANDALF module can be used as a 128-channel pattern generator for testing the multichannel TDC's functionality such as time resolution, differential nonlinearity or the rate capability. Future work concentrates on a significant improvement of the time resolution. It is planned to double the number of phase shifted clocks and to increase the overall clock frequency to reduce the LSB size to less than 150ps.

Author: Mr BUECHELE, Maximilian (Physikalisches Institut der Albert-Ludwigs-Universitaet Freiburg)

Co-authors: Dr SCHILL, Christian (Physikalisches Institut der Albert-Ludwigs-Universitaet Freiburg); Mr HERRMANN, Florian (Physikalisches Institut der Albert-Ludwigs-Universitaet Freiburg); Prof. FISCHER, Horst (Physikalisches Institut der Albert-Ludwigs-Universitaet Freiburg); Prof. KOENIGSMANN, Kay (Physikalisches Institut der Albert-Ludwigs-Universitaet Freiburg); Mr SCHOPFERER, Sebastian (Physikalisches Institut der Albert-Ludwigs-Universitaet Freiburg)

Presenter: Mr BUECHELE, Maximilian (Physikalisches Institut der Albert-Ludwigs-Universitaet Freiburg)

Session Classification: Posters

Track Classification: Logic