SLID-ICV interconnection technology for the ATLAS pixel upgrade at HL-LHC

Anna Macchiolo
L. Andricek, H.G. Moser, R. Nisius, R.H. Richter, P. Weigell
Max-Planck-Institut für Physik & MPI Halbleiterlabor (HLL)
Munich

In collaboration with Fraunhofer EMFT

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Benefits of vertical integration technology for HEP

Requirements for Pixel Upgrades at HL-LHC:

- Finer granularity to reduce occupancy and improve resolution → Multi-tier ASIC with Through Silicon Vias (Via first approach)
- Reduced material budget for better impact parameter resolution → thin sensors and ASIC
- Highly radiation resistant detectors → thinner sensors
- Larger fraction of active area → 4-side buttable ASIC with Via first or Via last approach
MPP 3D R&D Program: demonstrator module

- **Step I:**
  - ATLAS FE-I3 ASIC thinned to 200 µm
  - n-in-p pixel sensors of 75 µm active thickness
  - thin sensors / ASIC interconnection using SLID
  - No TSV, integrated fan-out on sensor for service connection

- **Step II:**
  - TSV etched in the read-out chip on the front-side on every wire bonding pad to route signal and services to the ASIC backside
  - ASIC thinned to 50 µm
  - thin sensors / ASIC interconnection using SLID
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Sensor thinning technology at MPP-HLL

- The process has been completed including step #4. The handle wafer has been used as a support during the ASIC interconnection phase. Backside etching demonstrated in other productions.

- Production characteristics:
  - 8 n-in-p 6” wafers with ATLAS FE-I3 compatible sensors
  - Different active thicknesses: 75μm and 150μm
  - Pre-irradiation characterization:
    - Excellent device yield (79/80)
    - Low currents (~10 nA /cm²)
    - Good HV behaviour ($V_{bd} >> V_{fd}$)

L. Andricek et al., doi:10.1016/j.nima.2010.04.087
Sensor thinning technology at MPP-HLL

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EMFT SLID Process

Metallization SLID (Solid Liquid Interdiffusion)

- Alternative to bump bonding (less process steps “lower cost” (EMFT)).
- Small pitch possible (~ 20 \( \mu \text{m} \), depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

- However: no rework possible.
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Aim: determine the feasibility of the SLID interconnection within the parameters we need for the ATLAS pixels.

SLID efficiencies measured with daisy chains structures (wafer to wafer connections).

<table>
<thead>
<tr>
<th>Pad width [(\mu m^2])</th>
<th>Pitch [(\mu m])</th>
<th>Aplanarity</th>
<th>SLID Inefficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>30x30</td>
<td>60</td>
<td>0</td>
<td>&lt;1.2(\times10^{-4})</td>
</tr>
<tr>
<td>80x80</td>
<td>115</td>
<td>0</td>
<td>&lt;8.9(\times10^{-4})</td>
</tr>
<tr>
<td>80x80</td>
<td>100</td>
<td>0</td>
<td>&lt;7.8(\times10^{-4})</td>
</tr>
<tr>
<td>27x60</td>
<td>50,400</td>
<td>0</td>
<td>(5\pm1) (\times10^{-4})</td>
</tr>
<tr>
<td>30x30</td>
<td>60</td>
<td>100 nm</td>
<td>(10\pm4) (\times10^{-4})</td>
</tr>
<tr>
<td>30x30</td>
<td>60</td>
<td>1 (\mu m)</td>
<td>(4\pm3) (\times10^{-4})</td>
</tr>
</tbody>
</table>

A. Macchiolo et al. "Application of a new interconnection technology for the ATLAS pixel upgrade at SLHC"

Chip to wafer SLID interconnection (with handle wafer)

The chips on the handle wafer suffer from strong misalignment with respect to the nominal positions.
Chip to wafer SLID interconnection (with handle wafer)

After SLID interconnection and handle wafer removal
Chip to wafer SLID interconnection (with handle wafer)

FE-I3 chips (mostly not electrically functioning) used to improve the pressure homogeneity on the wafer during the SLID interconnection.
### Measured misalignment

Residual misalignment in the FE-I3 chips after correction for a global offset of the FE-I3 chips.

<table>
<thead>
<tr>
<th>Chip</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Δx [μm]</td>
<td>-23</td>
<td>44</td>
<td>-34</td>
<td>-8</td>
<td>-16</td>
<td>-17</td>
<td>-17</td>
<td>-16</td>
</tr>
<tr>
<td>Tilt [°]</td>
<td>-0.38</td>
<td>0.72</td>
<td>-0.61</td>
<td>-0.21</td>
<td>-0.21</td>
<td>-0.23</td>
<td>-0.24</td>
<td>-0.26</td>
</tr>
<tr>
<td>Pad size</td>
<td>27</td>
<td>60</td>
<td>23</td>
<td>29</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distance</td>
<td>60</td>
<td>29</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- 5 modules with a misalignment and tilt that do not induce shorts or open, included the area in the corners.
- Very good alignment for the SLID pads in the central region of the FE-I3 matrix.
SLID Module measurements

- SLID modules glued and wire-bonded to a modified version of the ATLAS pixel detector board (Bonn University)
- Measurements performed with the ATLAS USBPix read-out system
Overview of the 5 SLID modules tested

- The five sensors and the chips are all functional
- Leakage current below 100 nA for all SCMs
- Breakdown voltages exceed 120V – full depletion around 40V
- Chips can be tuned between 2500 and 3500 e with a small threshold dispersion
- The charge collection with $^{90}$Sr source scans homogenous over the five devices
\( ^{90} \text{Sr} \) Source Scans before irradiation

- Collected Charge with \( ^{90} \text{Sr} \): compatible with the signal from bump-bonded n-in-p module, 300 \( \mu \text{m} \) thick, after scaling for the active thickness.

\[ d_{\text{active}} = 75 \ \mu \text{m} \]

MPV \( = 4.6 \text{ ke}^- \)
Performance after irradiation

- SCMs irradiated to $2 \times 10^{15} \text{n}_{eq.}/\text{cm}^2$ with reactor neutrons in Ljubljana
- Tuned threshold of 2500 e, Noise of 170 e
- MPV of collected charge constant above 200V

Charge before irradiation

Number of unconnected channel stable after irradiation and multiple thermal cycle (+$20^\circ\text{C} \rightarrow -30^\circ\text{C}$)

SLID interconnection is radiation hard and withstands thermal cycling
Overview of interconnection efficiency

<table>
<thead>
<tr>
<th>Chip</th>
<th>Uncon. Pixels</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>731</td>
<td>30</td>
</tr>
<tr>
<td>7</td>
<td>713</td>
<td>29</td>
</tr>
<tr>
<td>8</td>
<td>274</td>
<td>11</td>
</tr>
<tr>
<td>9</td>
<td>134</td>
<td>6</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

90Sr scan

Connected channel

Unconnected channel
Problem with contact opening in BCB passivation

- BCB (BenzoCycloButhene) passivation deposited to planarize the sensor surface before Cu and Sn electroplating

- Badly defined BCB contact openings observed in 2 sensor wafers not yet electroplated → pattern fully compatible with the distribution of unconnected channels in the modules

Unconnected channels are not an intrinsic SLID problem!
Possible solution to the BCB contacts problem

- Applied at IZM Berlin a descum process in a SF$_6$ plasma to clean and increase the openings

- An optical inspection has shown that the contacts have improved all over the pixel structures

- Process performed on the sensor wafers to be interconnect to the chips with TSV after electroplating
Connection strength – Pull out tests

- Pull out test performed with “mechanical” chips placed below the hot chips
- Connection strength of the order of 0.01N → similar to bump-bonding and other pixel interconnection technology
Through Silicon Vias processing

SACVD Pad Planarization, TSV Litho, Etching with Bosch process, cross section \( \sim 4 \times 10 \ \mu m^2 \), depth=60 \( \mu m \)

TSV Isolation with SACVD \( SiO_2 \) \( \sim 300 \ nm \)

TSV Filling with TiN seed + CVD W

Electroplating of Cu on the front side

Bonding to handling substrate, thinning to 50 \( \mu m \)

Exposure of W in TSV and Alu spattering for creation of pads on the back-side
Through Silicon Vias processing

ICV-Dimensions:
3 μm x 10 μm x 50 μm

300 nm SACVD TEOS
20 nm TiN CVD
900 nm W CVD und W Backetch
800 nm M1 (AlSiCu, structured)
850 nm PN/POX (Passivation)

Trench #11

10 μm

Courtesy of R. Wieland, EMFT
TSV in the FE-I3 chips

- First etching trials on dummy wafer
  - Performed in the un-thinned FE-I3 chips of one designated test-wafer
  - Etched to a depth of ~ 60 µm
  - Optimize the trench width to obtain the same depth as in the TSV

- Process plan of the hot FE-I3 wafer
  - Local planarisation of the fan-out pads by depositing and etching of SACVD-Oxide
    - Perform via etching and filling in the hot FE-I3 wafer
  - Connect the readout chip with SLID to the hot sensor wafers
Summary and Outlook

- FE-I3 modules functional after SLID Interconnection, with extremely good performance (low noise, threshold dispersion, charge collection) before and after irradiation
  - SLID withstands thermal cycling
    - Challenging chip alignment on the handle wafer
  - Systematic increase of not connected channels for a fraction the modules close to the wafer center due to the BCB contact opening, not related to the interconnection technology

Plans

- Optimize pick and place of the chips on handle wafer with new machines
  - Full SLID assembly of sensors and FE-I3 chips with TSV
  - Test the TSV approach on new ATLAS FE-I4 chip
Back-up Slides
Thin pixels for the ATLAS pixel Upgrade

- ATLAS pixel system for the Phase 2 Upgrade: In the inner layers radiation doses of $1\text{--}2\times10^{16} \text{n_{eq}/cm}^2$ are foreseen

- Higher electric fields in thinner devices at equal $V_{\text{bias}}$ : at HL-LHC fluences higher CCE is expected (larger drift velocity, charge multiplication)

- Minimize material and multiple scattering

Charge collection efficiency measured with thin p-type strip sensors produced by MPP-HLL – Alibaba read-out system

![Graph showing charge collection efficiency for different active thicknesses and doping densities.]
SLID Module 9: chip tuning

- Pixel with lower noise are an indication of unconnected channels

**Threshold tuned to 2800 e⁻**

**Unconnected channels:**

**Threshold noise**
Connection map of SLID 7 module

Column #

Row #

connected
don't connected
Causes of SLID inefficiency – BCB openings

- BCB passivation not completely open
New daisy chain production for SLID testing

- FE-I4 geometry, daisy chains with 26800 pads each
- Arranged in the most regular pattern possible
- Test of the placement on the handle wafer with new flip-chipping machine at EMFT
- SLID efficiency with measurements of the electrical continuity

EMFT can do the copper electroplating in house, tin will be available in October (subcontracted to IZM Berlin in the past).
SLID Module 9: Charge Collection

- Number of unconnected channels ~ 6%
- The module is fully functional except for the fraction of disconnected channel
- Similar results for SLID8-SLID7-SLID6 with an increasing number of unconnected channels.