SLID-ICV interconnection technology for the ATLAS pixel upgrade at HL-LHC

Anna Macchiolo

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In collaboration with Fraunhofer EMFT

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Benefits of vertical integration technology for HEP

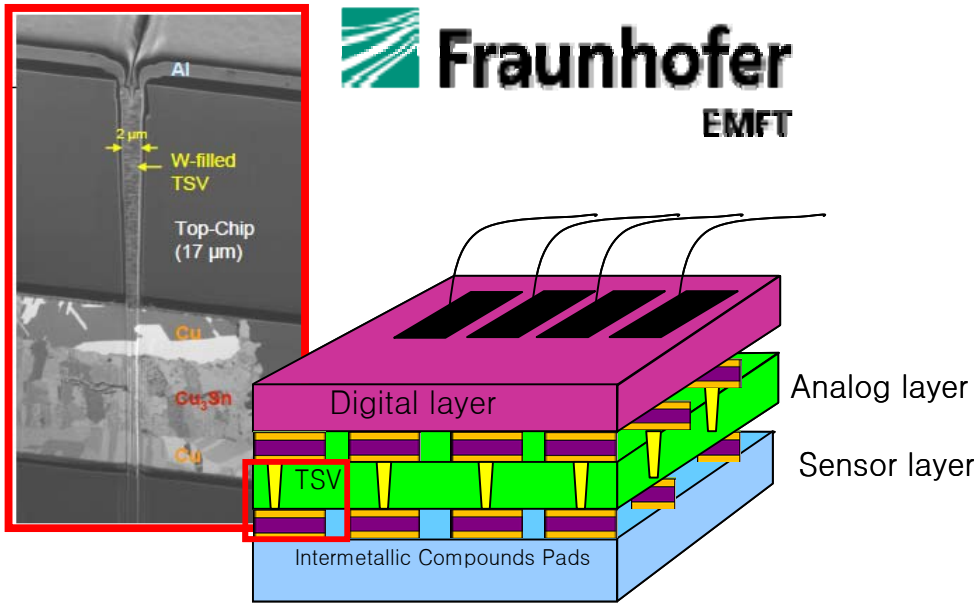
- Requirements for Pixel Upgrades at HL-LHC:

Finer granularity to reduce occupancy and improve resolution → Multi-tier ASIC with Through Silicon Vias (Via first approach)

Reduced material budget for better impact parameter resolution → thin sensors and ASIC

Highly radiation resistant detectors → thinner sensors

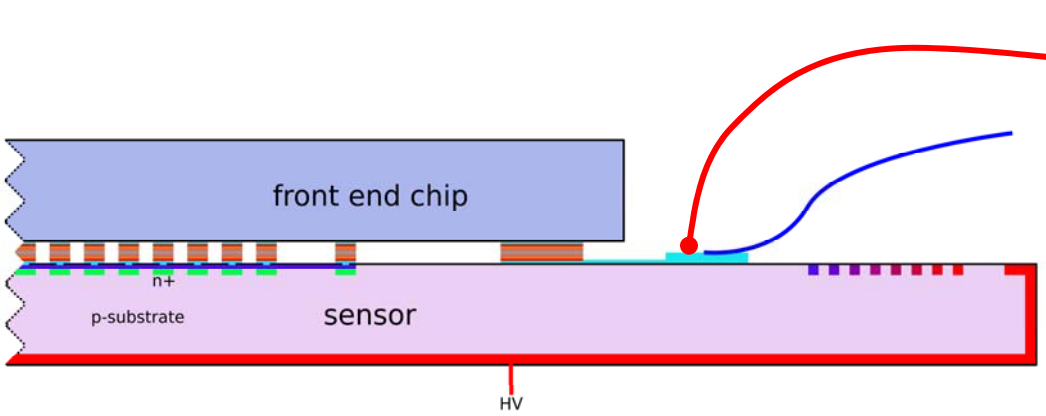
Larger fraction of active area → 4-side buttable ASIC with Via first or Via last approach

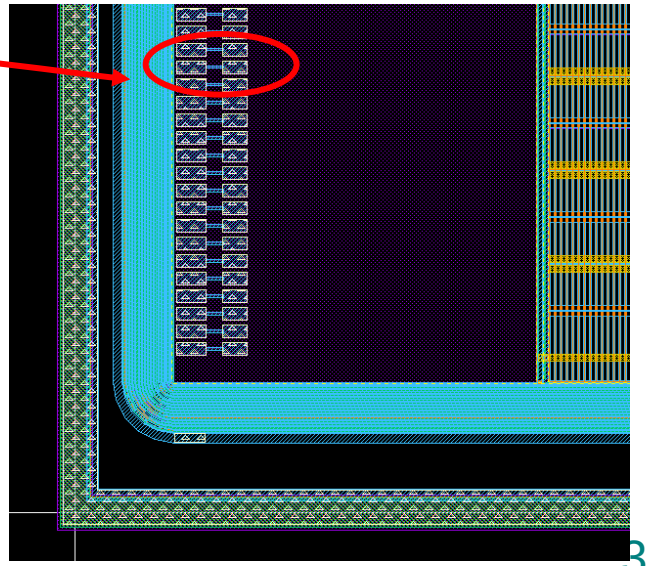


MPP 3D R&D Program: demonstrator module

- Step I:
  - ATLAS FE-I3 ASIC thinned to 200 μm
  - n-in-p pixel sensors of 75 μm active thickness
  - thin sensors / ASIC interconnection using SLID
  - No TSV, integrated fan-out on sensor for service connection

- Step II:
  - TSV etched in the read-out chip on the front-side on every wire bonding pad to route signal and services to the ASIC backside
  - ASIC thinned to 50 μm
  - thin sensors /ASIC interconnection using SLID





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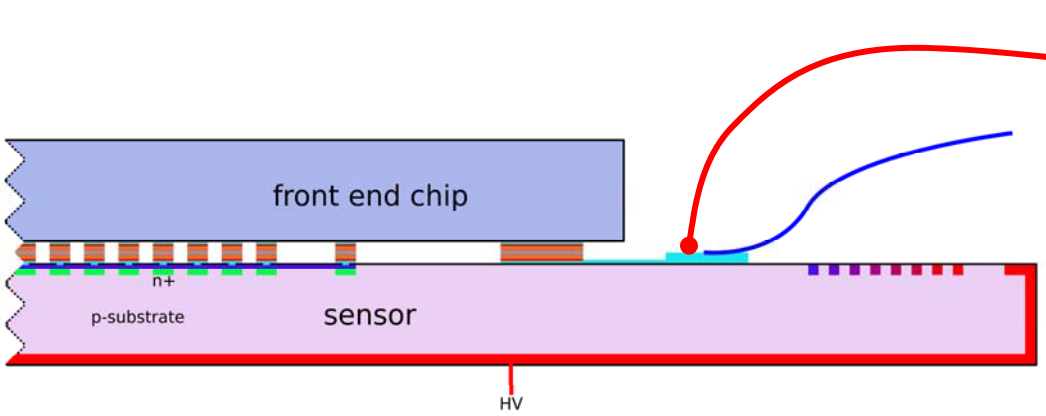

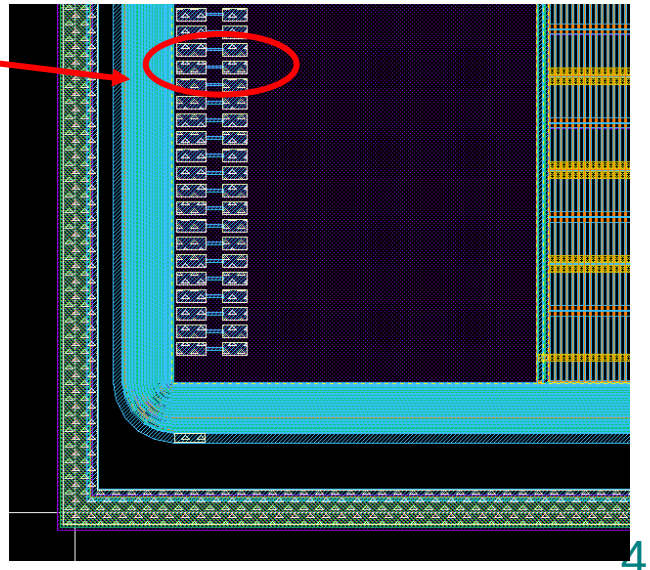

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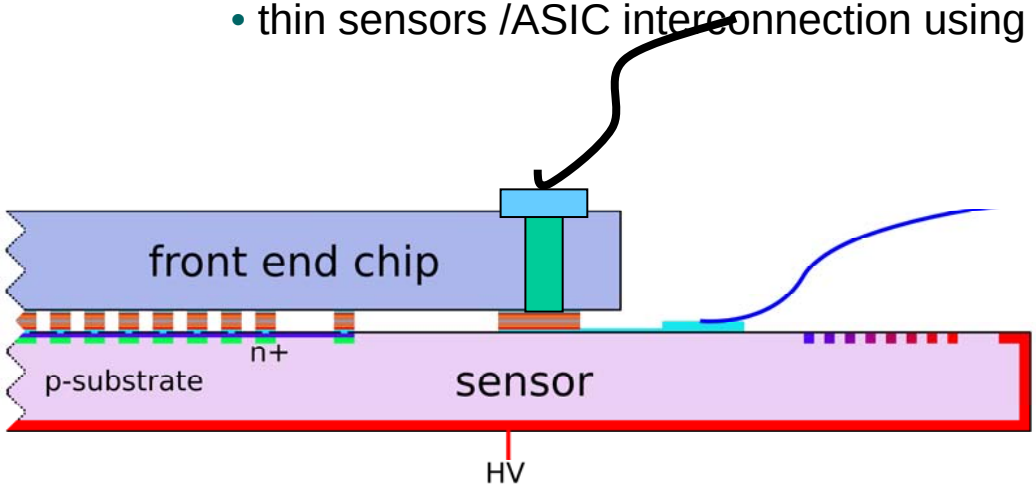
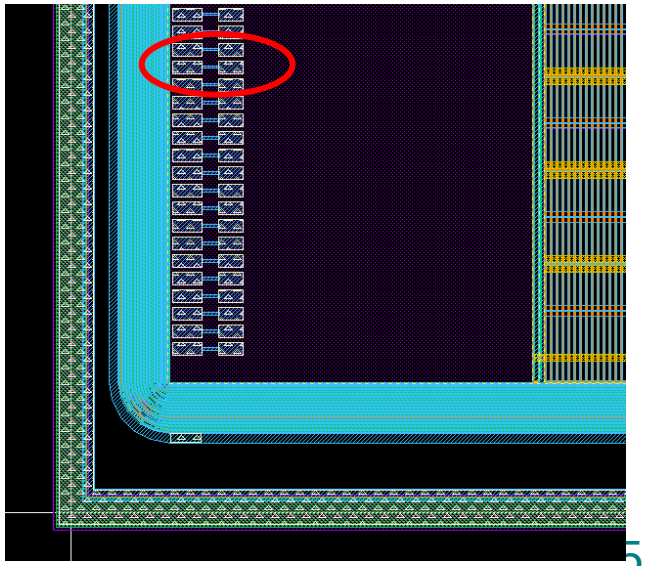
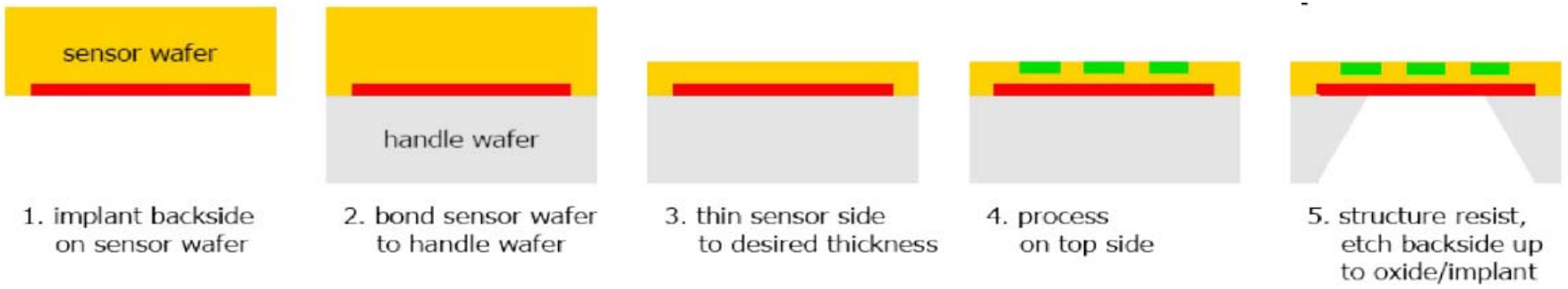
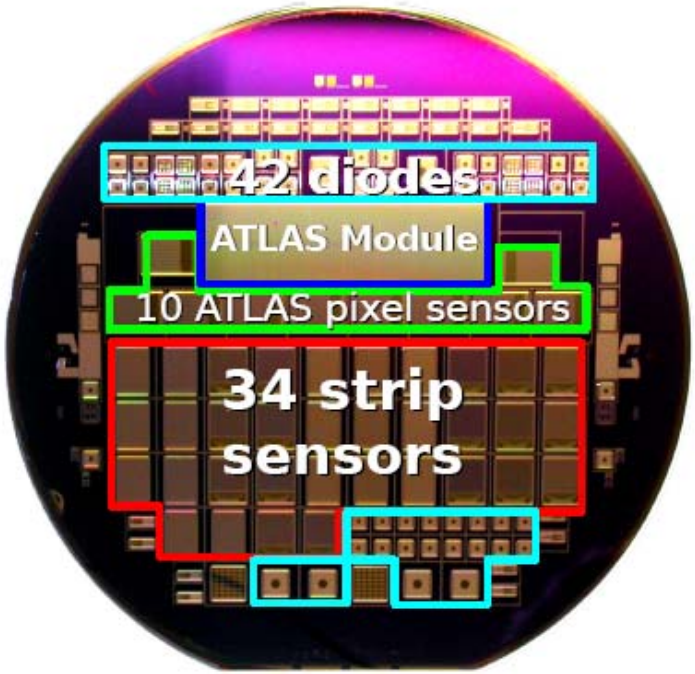




Sensor thinning technology at MPP-HLL



➢ The process has been completed including step #4. The handle wafer has been used as a support during the ASIC interconnection phase. Backside etching demonstrated in other productions

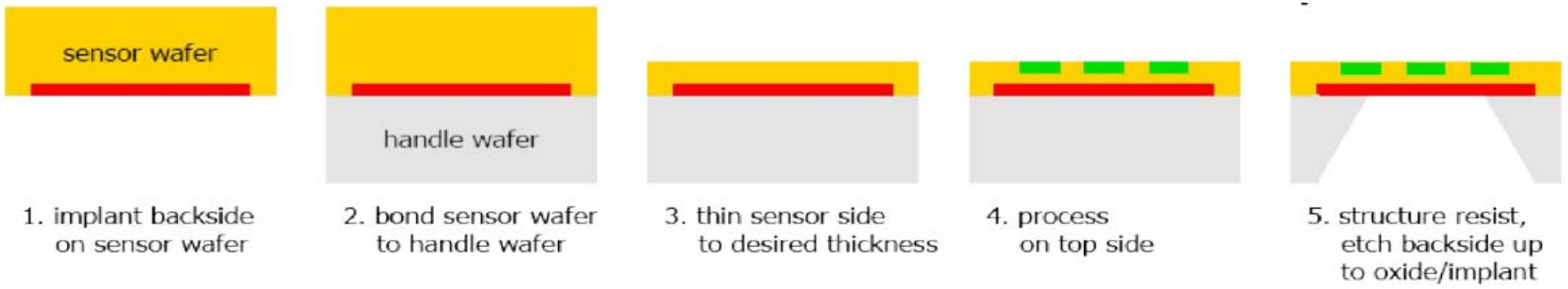


➢ Production characteristics:

- 8 n-in-p 6“ wafers with ATLAS FE-I3 compatible sensors
- Different active thicknesses: 75µm and 150µm
- Pre-irradiation characterization:
  - Excellent device yield (79/80)
  - Low currents (~10 nA /cm^2)
  - Good HV behaviour (V_{bd} >>V_{fd})

L. Andricek et al., doi:10.1016/j.nima.2010.04.087

Sensor thinning technology at MPP-HLL



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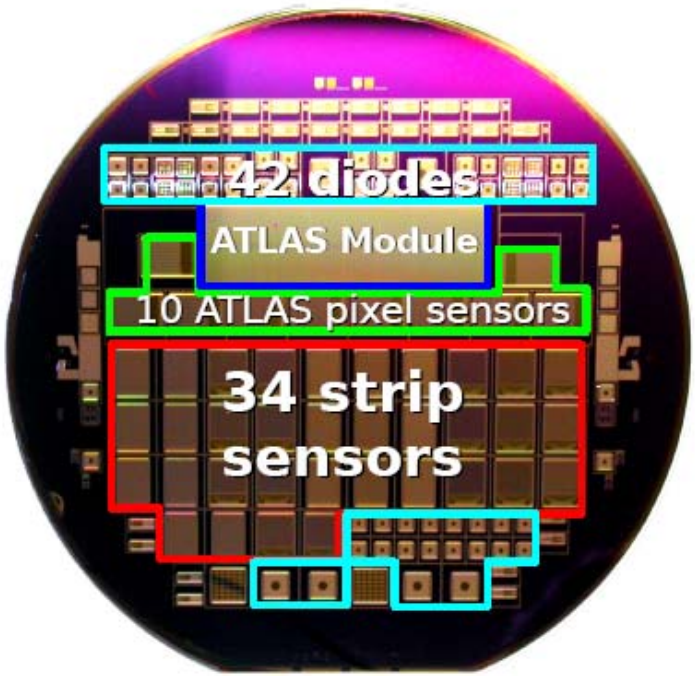
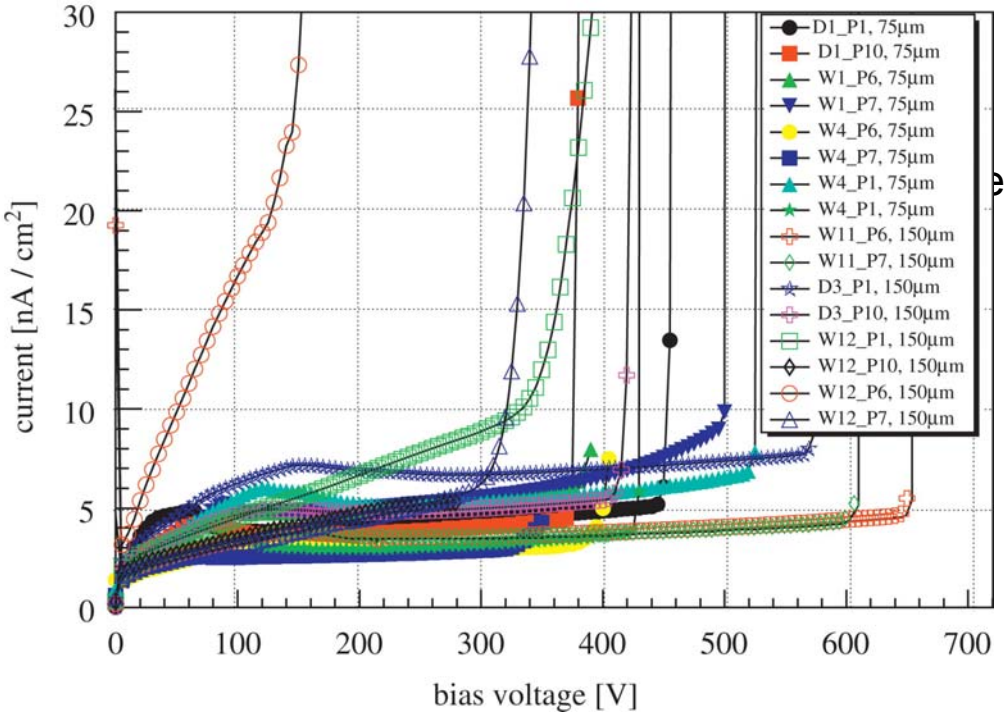
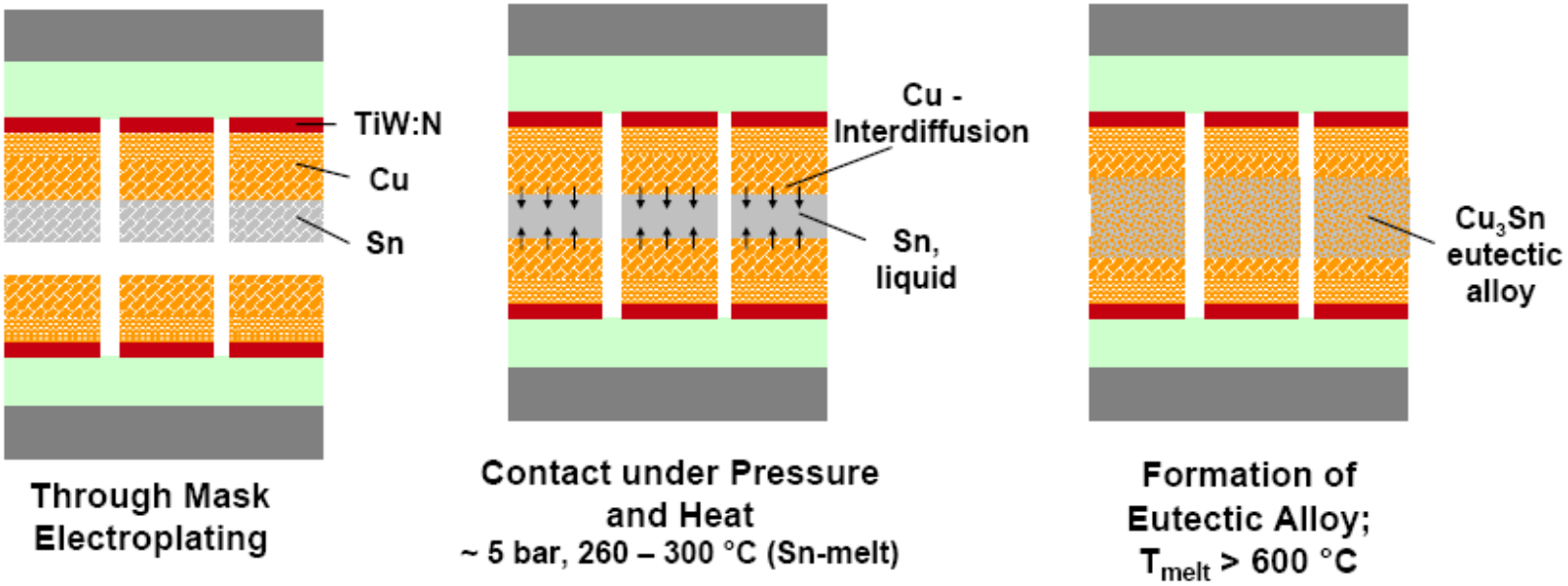




EMFT SLID Process

Metallization SLID (Solid Liquid Interdiffusion)



- Alternative to bump bonding (less process steps “lower cost” (EMFT)).
- Small pitch possible (~ 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

- However: no rework possible.

Fraunhofer EMFT

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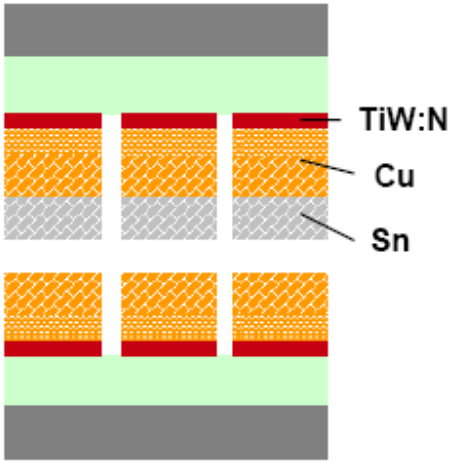
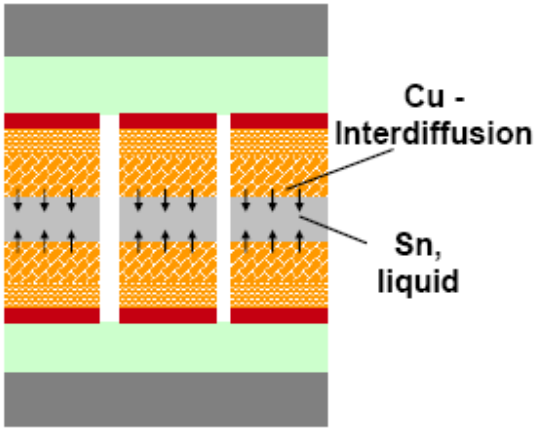
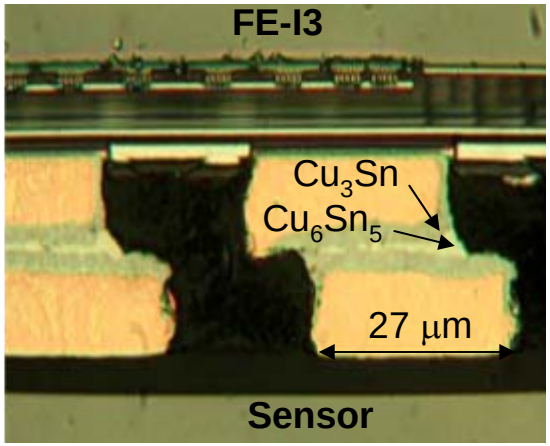


Through Mask Electroplating



Contact under Pressure and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)



Formation of Eutectic Alloy;
T_{melt} > 600 °C

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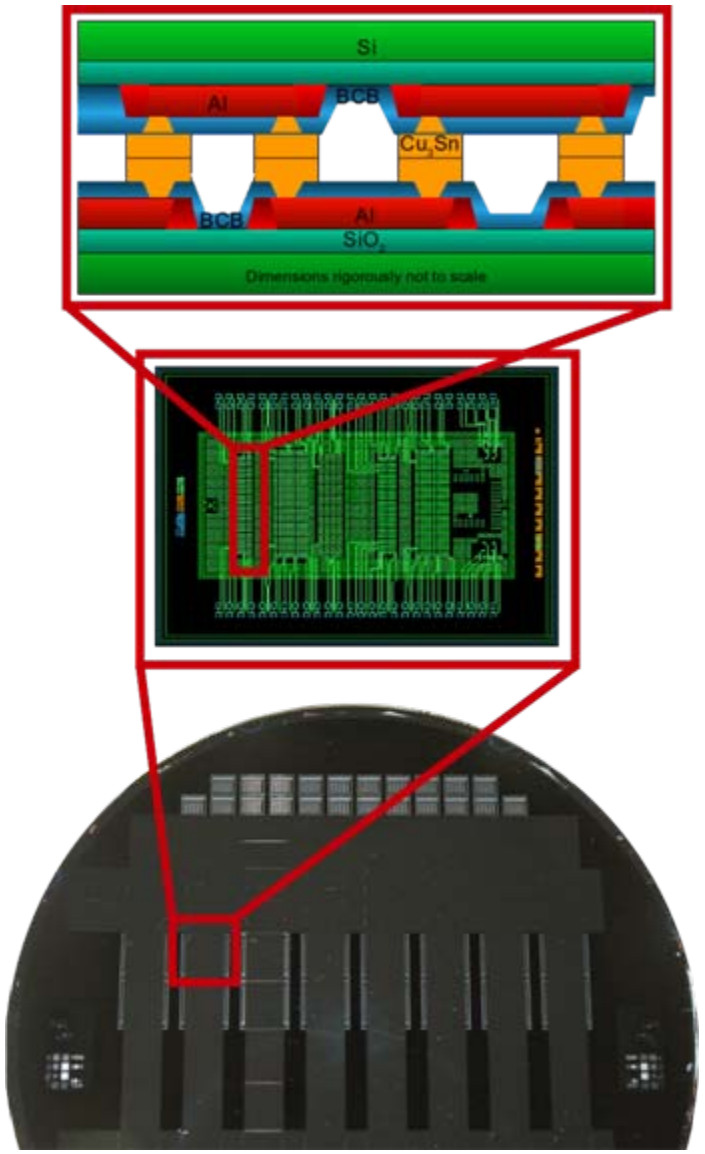
Fraunhofer EMFT

Daisy chains: wafer-to-wafer SLID



- Aim: determine the feasibility of the SLID inter-connection within the parameters we need for the ATLAS pixels.

- SLID efficiencies measured with daisy chains structures (wafer to wafer connections).

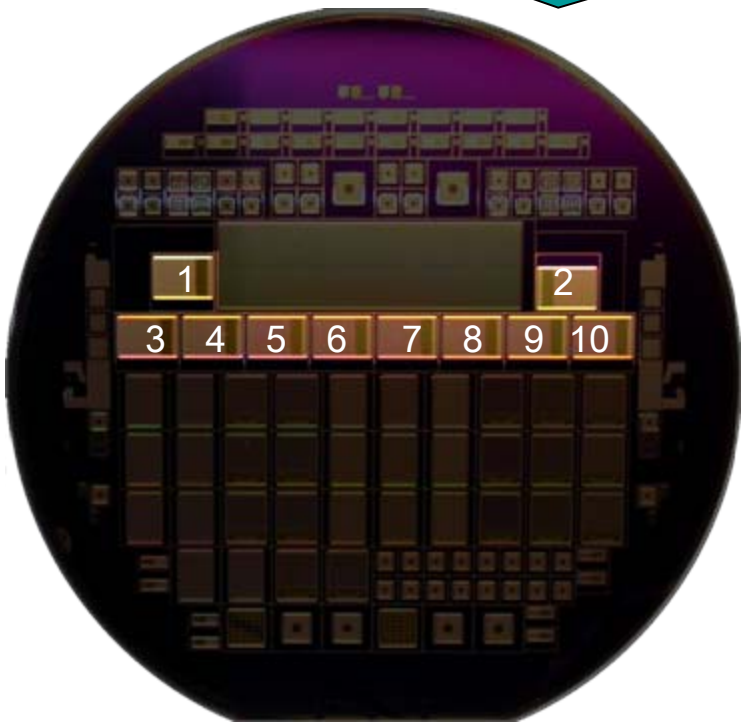
Pad width [μm²]	Pitch [μm]	Aplanarity	SLID Inefficiency
30x30	60	0	$<1.2\times10^{-4}$
80x80	115	0	$<8.9\times10^{-4}$
80x80	100	0	$<7.8\times10^{-4}$
27x60	50,400	0	$(5\pm1)\times10^{-4}$
30x30	60	100 nm	$(10\pm4)\times10^{-4}$
30x30	60	1 μm	$(4\pm3)\times10^{-4}$

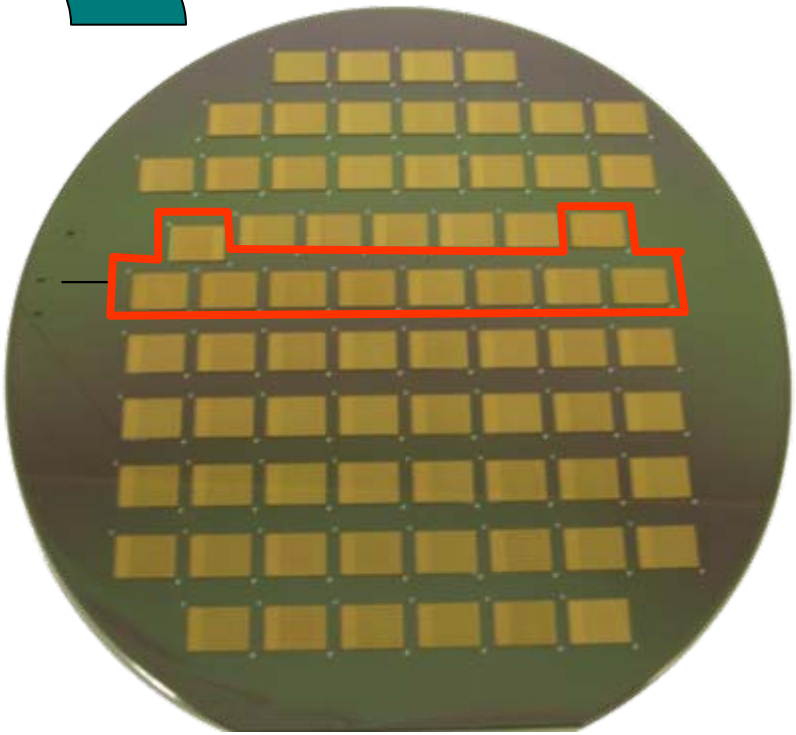
A. Macchiolo et al. “Application of a new interconnection technology for the ATLAS pixel upgrade at SLHC“
http://cdsweb.cern.ch/record/1234896/files/p216.pdf

Chip to wafer SLID interconnection (with handle wafer)

Sensor wafer
75 μm active thickness

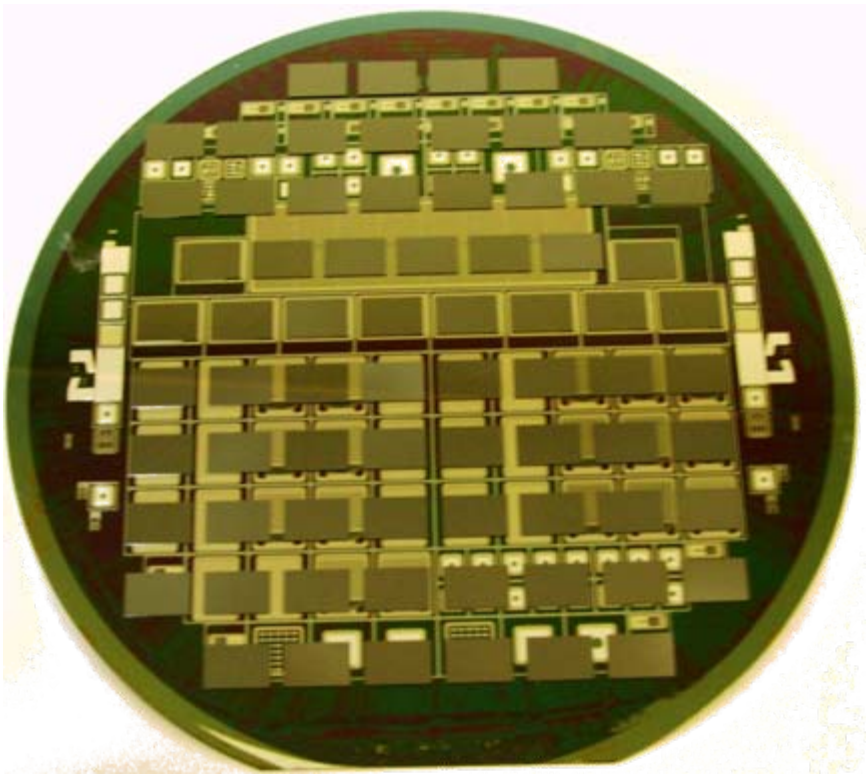
FE-I3 chips reconfigured on a 6" handle wafer





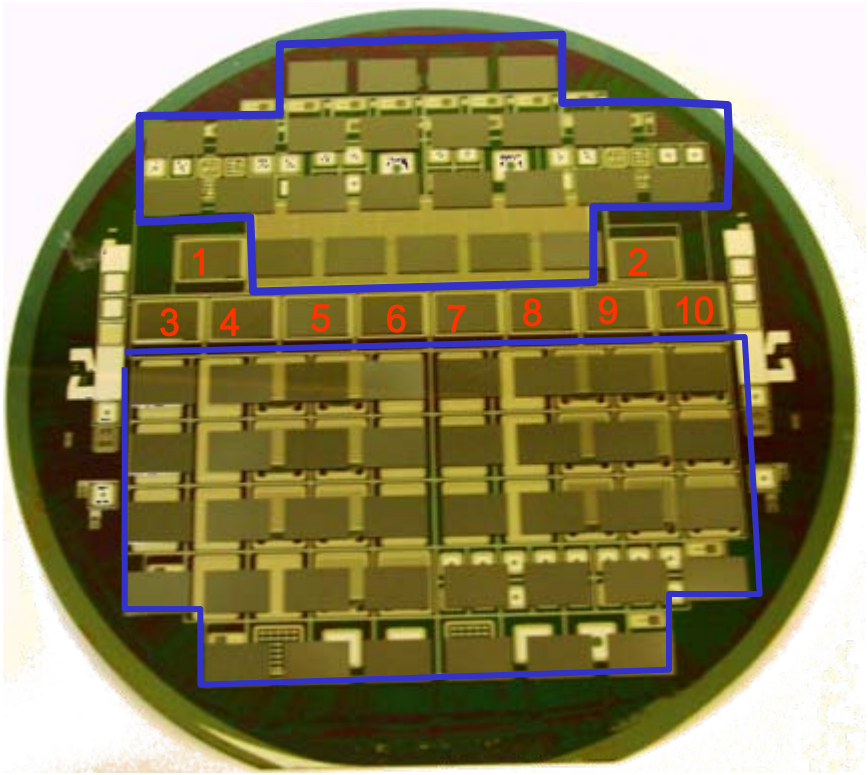
The chips on the handle wafer suffer from strong misalignment with respect to the nominal positions.

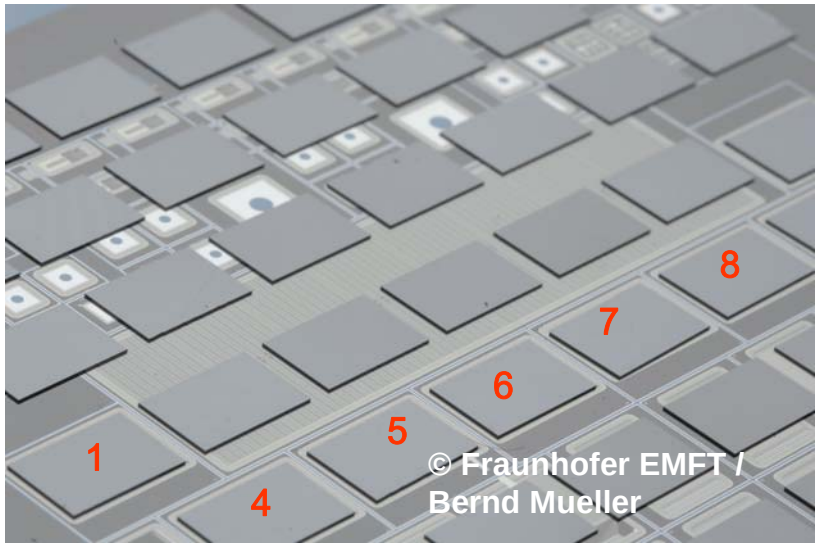
Chip to wafer SLID interconnection (with handle wafer)



After SLID interconnection and handle wafer removal

Chip to wafer SLID interconnection (with handle wafer)





FE-I3 chips (mostly not electrically functioning) used to improve the pressure homogeneity on the wafer during the SLID interconnection

Measured misalignment

1 ★

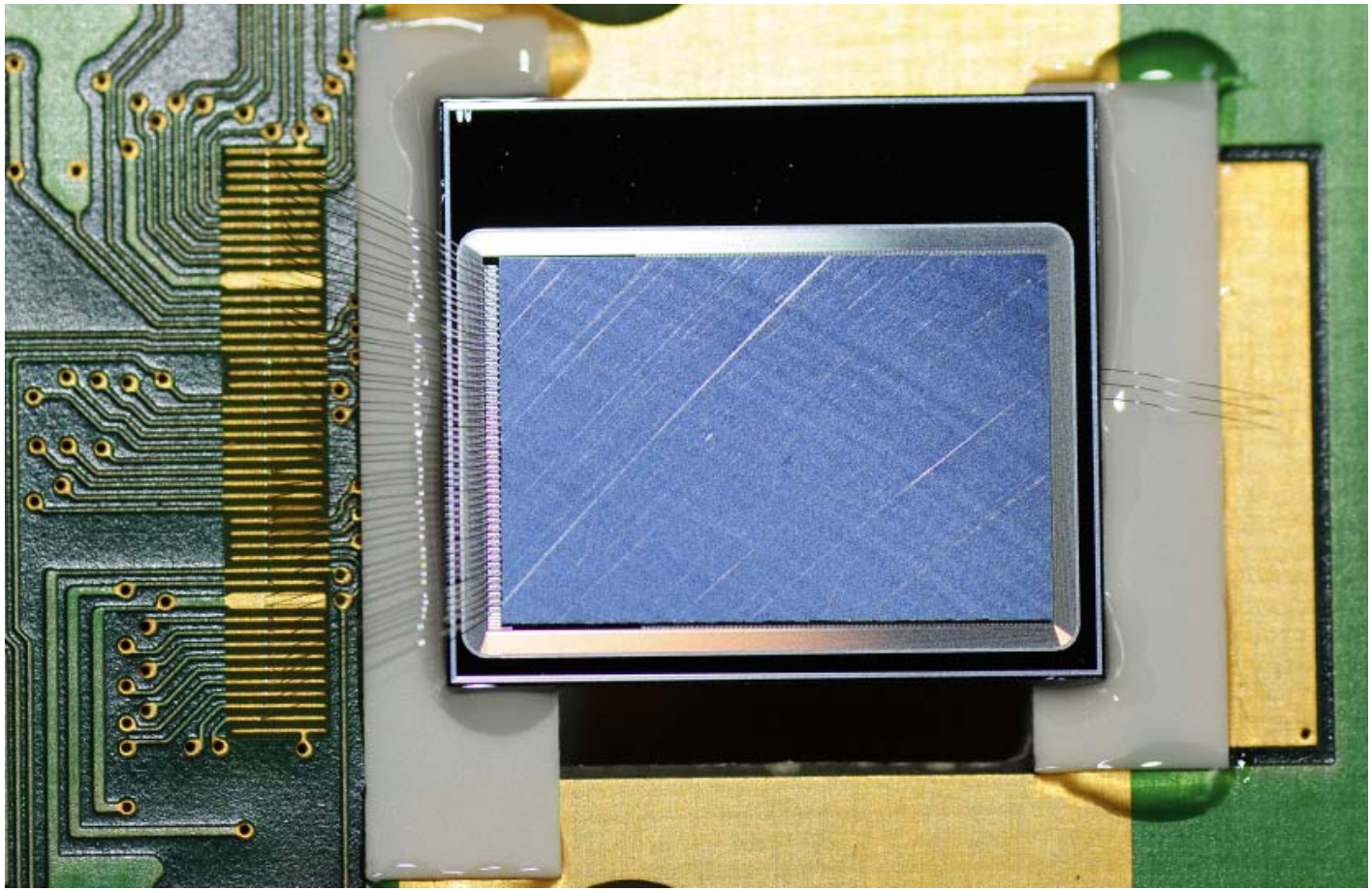
Residual misalignment in ★ after correction for a global offset of the FE-I3 chips

Chip	3	4	5	6	7	8	9	10	Pad size	Distance
Δx [μm]	-23	44	-34	-8	-16	-17	-17	-16	27	23
Δy[μm]	-34	73	-58	-19	-18	-25	-21	-25	60	29
Tilt [°]	-0.38	0.72	-0.61	-0.21	-0.21	-0.23	-0.24	-0.26		

- 5 modules with a misalignment and tilt that do not induce shorts or open, included the area in the corners
- Very good alignment for the SLID pads in the central region of the FE-I3 matrix

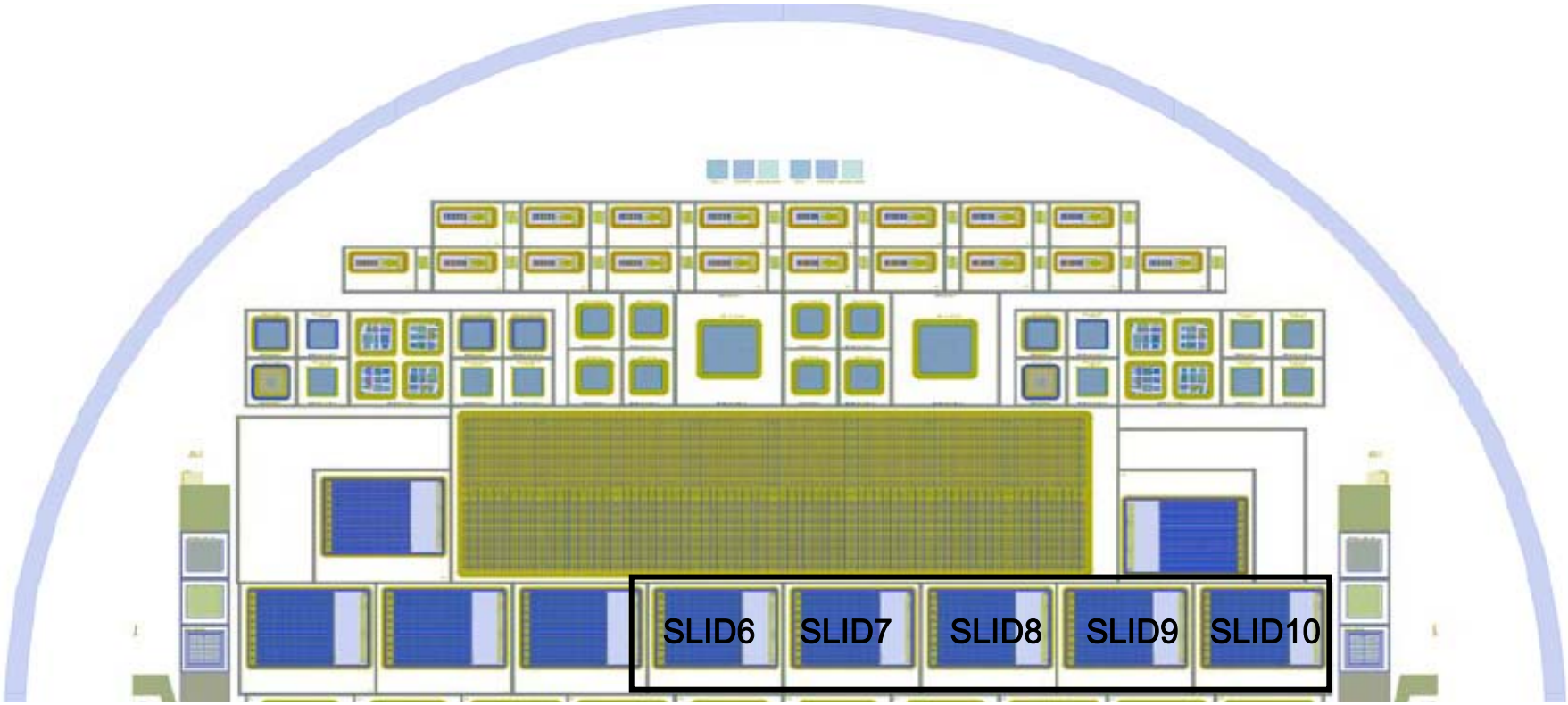
SLID Module measurements

- SLID modules glued and wire-bonded to a modified version of the ATLAS pixel detector board (Bonn University)
- Measurements performed with the ATLAS USBPix read-out system



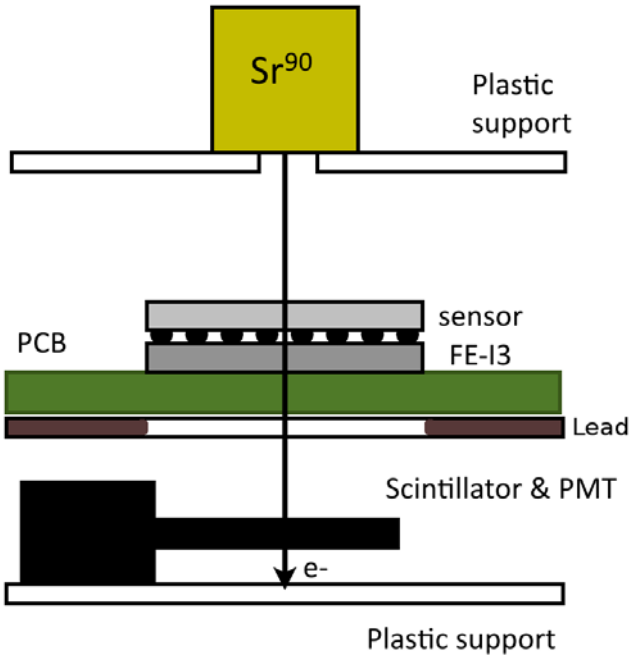
Overview of the 5 SLID modules tested

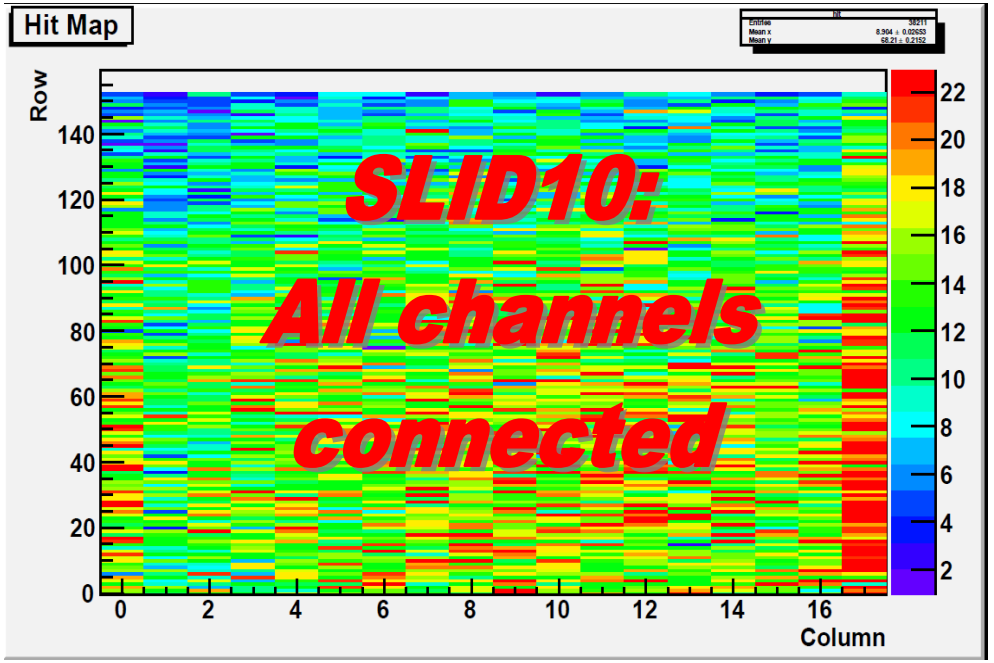
- The five sensors and the chips are all functional
- Leakage current below 100 nA for all SCMs
- Breakdown voltages exceed 120V – full depletion around 40V
- Chips can be tuned between 2500 and 3500 e with a small threshold dispersion
- The charge collection with ^{90}Sr source scans homogenous over the five devices

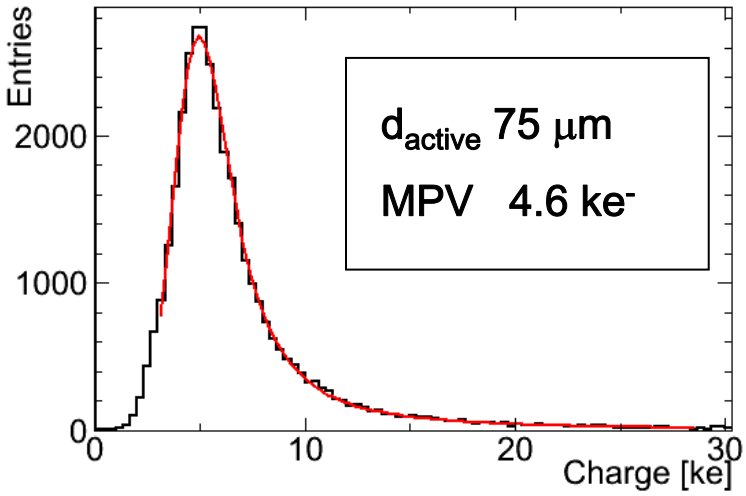


Modules tested

^{90}Sr Source Scans before irradiation



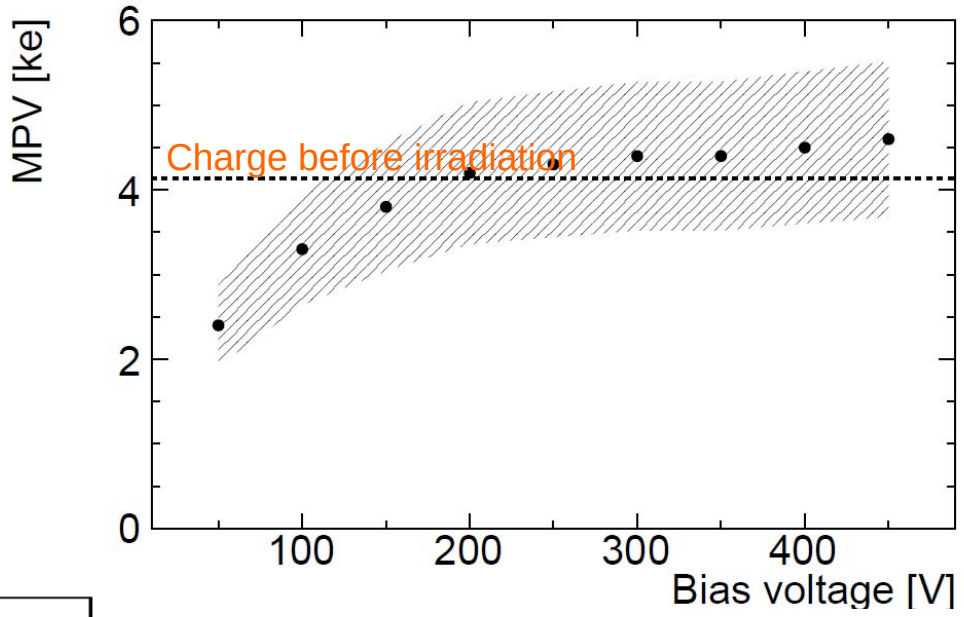


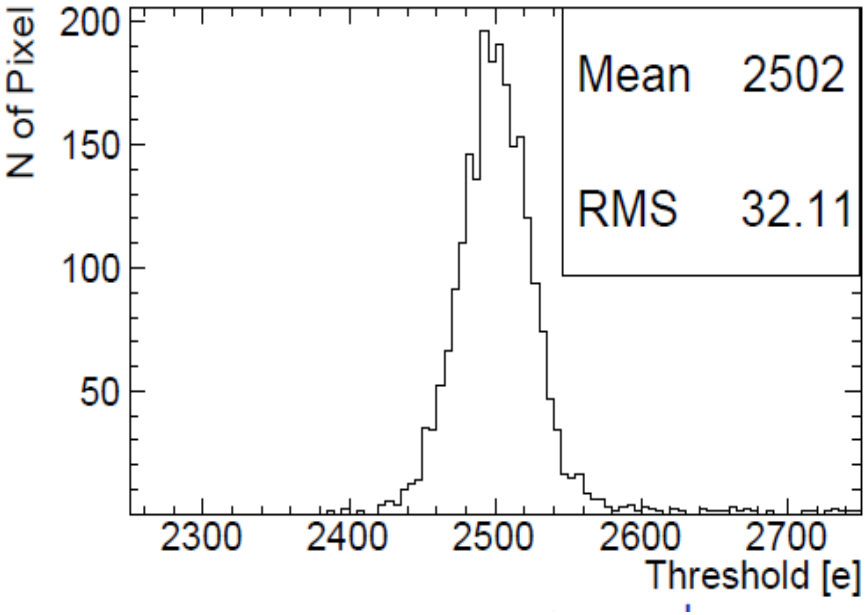


- Collected Charge with ^{90}Sr: compatible with the signal from bump-bonded n-in-p module, 300 um thick, after scaling for the active thickness

Performance after irradiation

- SCMs irradiated to 2×10^{15} n_{eq}./cm^2 with reactor neutrons in Ljubljana
- Tuned threshold of 2500 e, Noise of 170 e
- MPV of collected charge constant above 200V



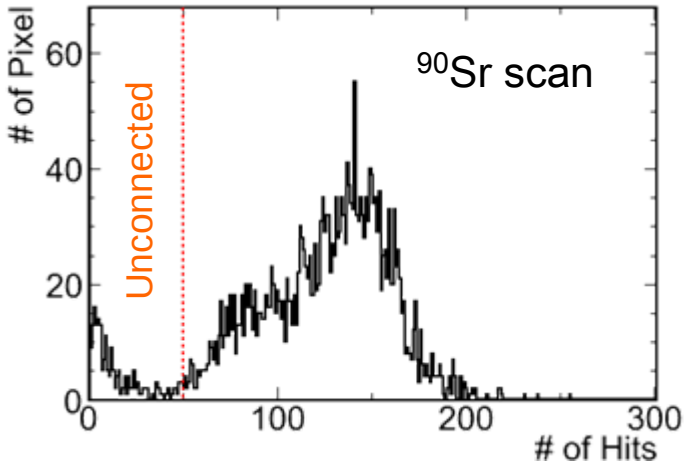


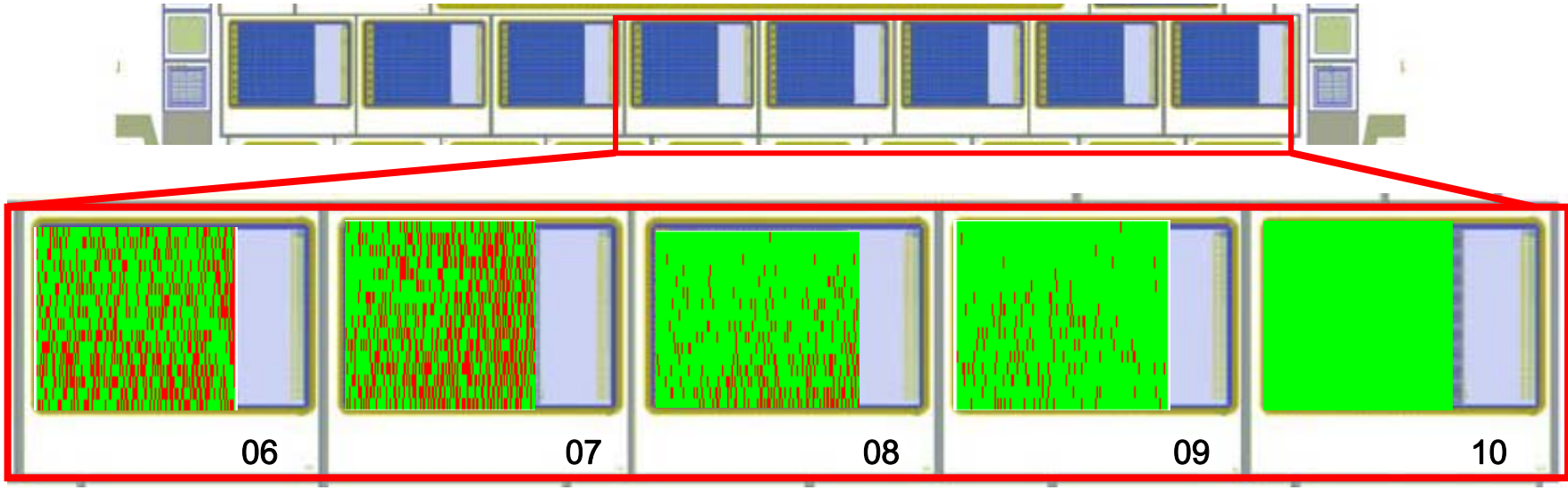
- Number of unconnected channel stable after irradiation and multiple thermal cycle (+20°C → -30°C)

SLID interconnection is radiation hard and withstands thermal cycling

Overview of interconnection efficiency

Chip	Uncon. Pixels	%
6	731	30
7	713	29
8	274	11
9	134	6
10	0	

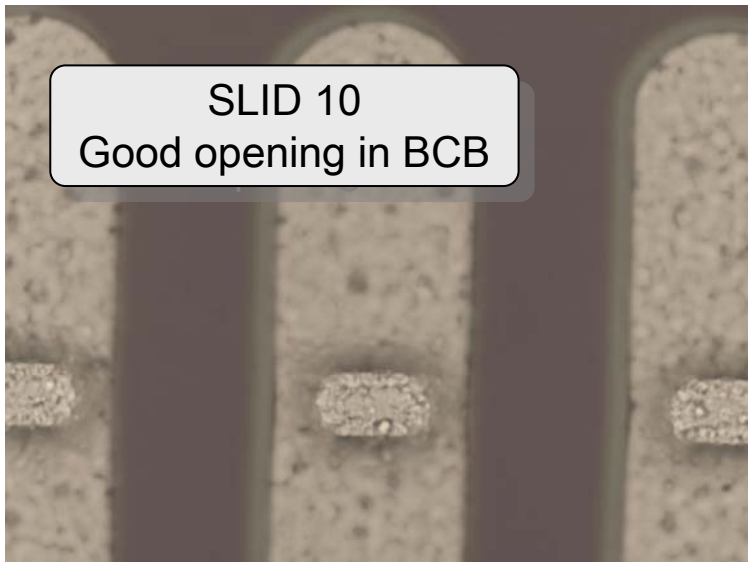




Connected channel

Unconnected channel

Problem with contact opening in BCB passivation

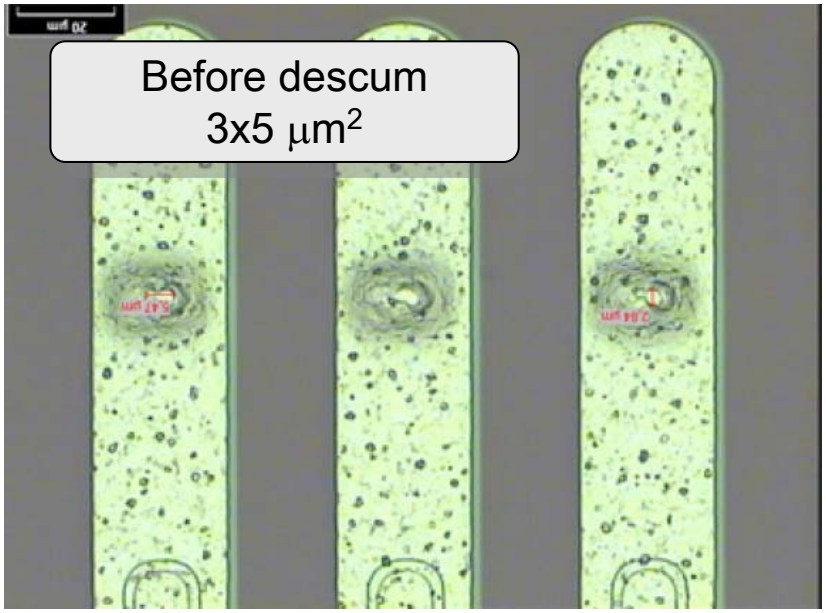


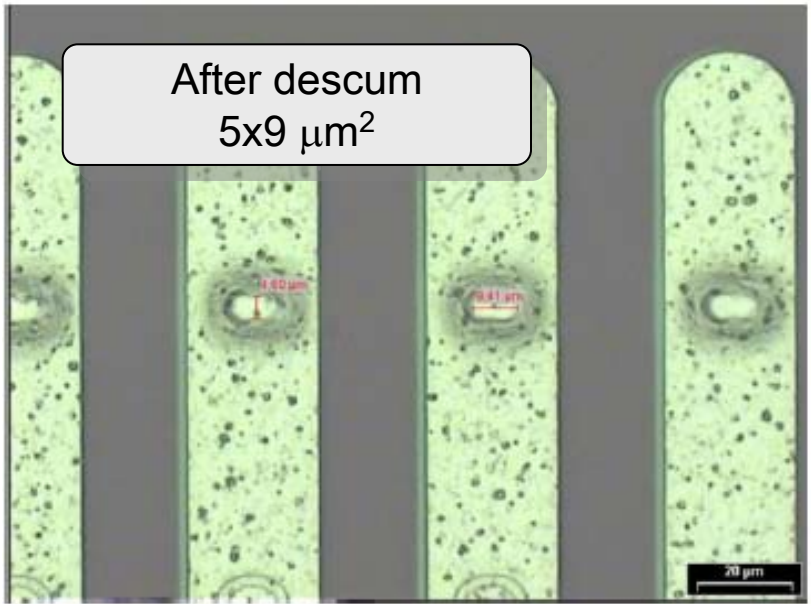
- BCB (BenzoCycloButhene) passivation deposited to planarize the sensor surface before Cu and Sn electroplating

- Badly defined BCB contact openings observed in 2 sensor wafers not yet electroplated → pattern fully compatible with the distribution of unconnected channels in the modules

Unconnected channels are not an intrinsic SLID problem!

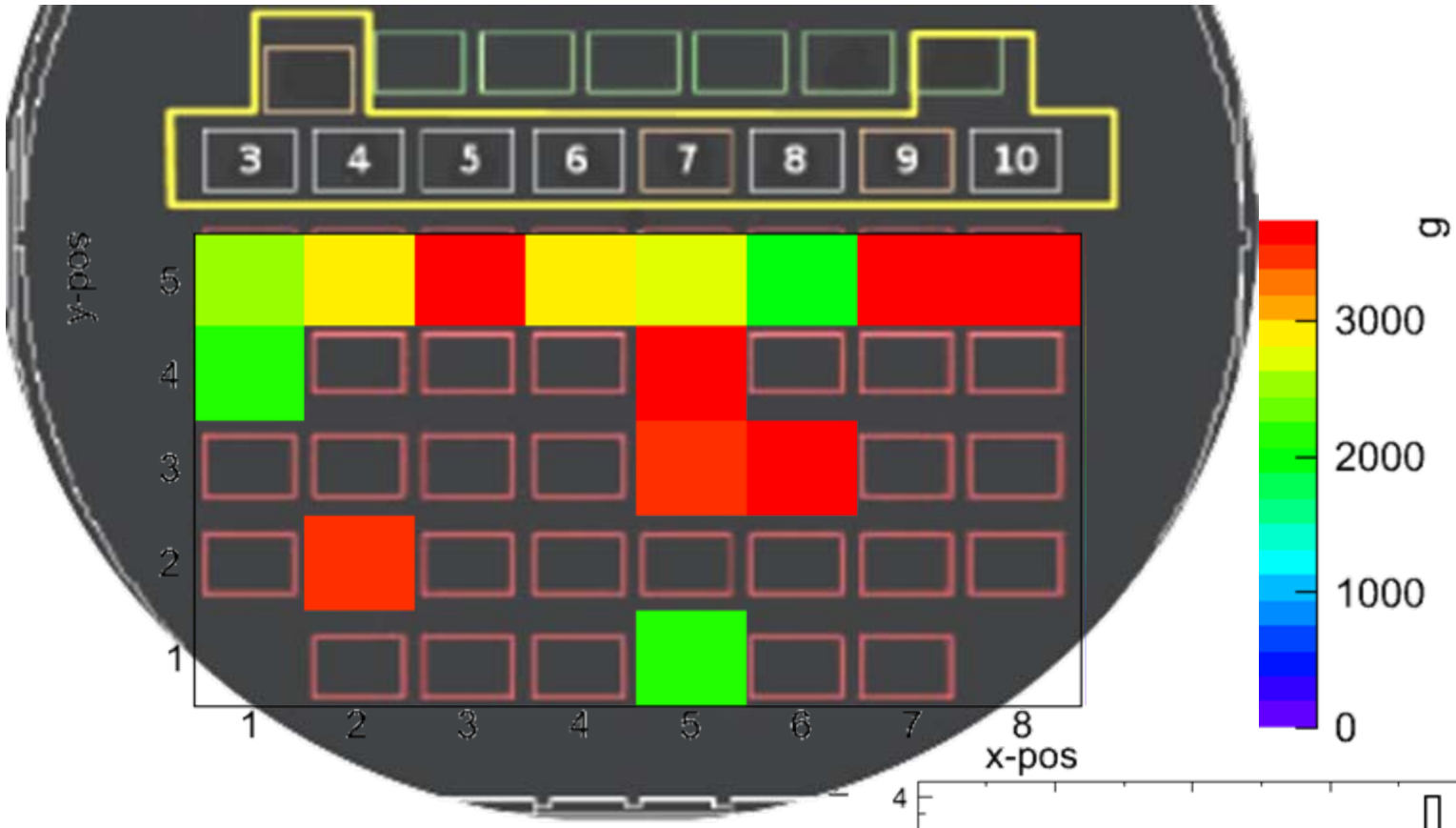
Possible solution to the BCB contacts problem



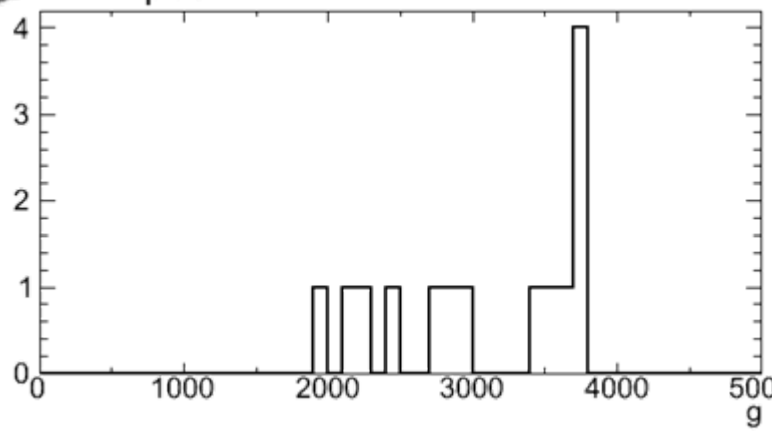


- Applied at IZM Berlin a descum process in a SF_6 plasma to clean and increase the openings
- An optical inspection has shown that the contacts have improved all over the pixel structures
- Process performed on the sensor wafers to be interconnect to the chips with TSV after electroplating

Connection strength – Pull out tests



- Pull out test performed with “mechanical” chips placed below the hot chips
- Connection strength of the order of 0.01N→ similar to bump-bonding and other pixel interconnection technology



Through Silicon Vias processing

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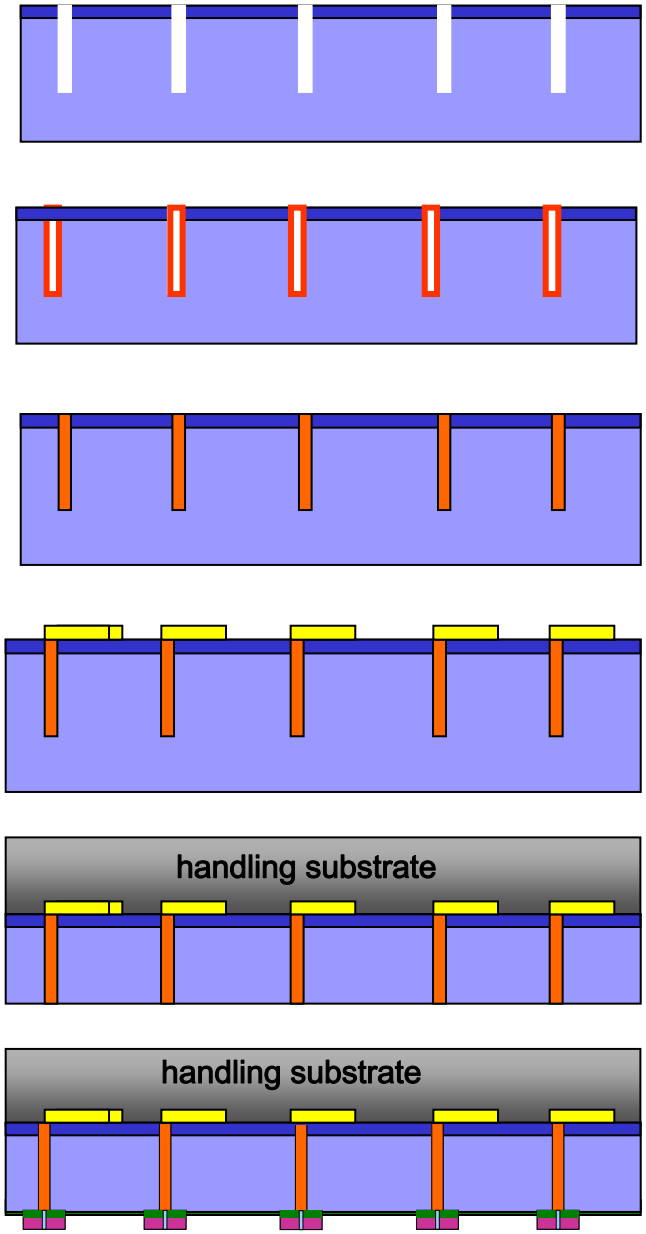
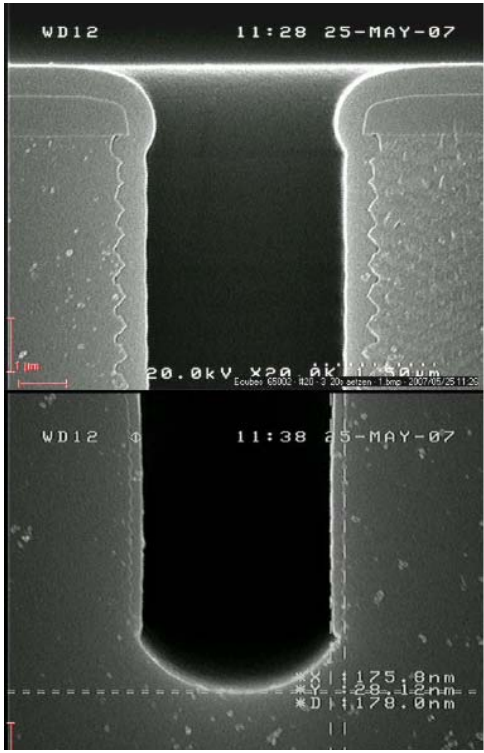


SACVD Pad Planarization, TSV Litho, Etching with Bosch process, cross section ~4x10 μm^2, depth=60 μm

TSV Isolation with SACVD SiO_2 ~ 300 nm

TSV Filling with TiN seed + CVD W

Electroplating of Cu on the front side

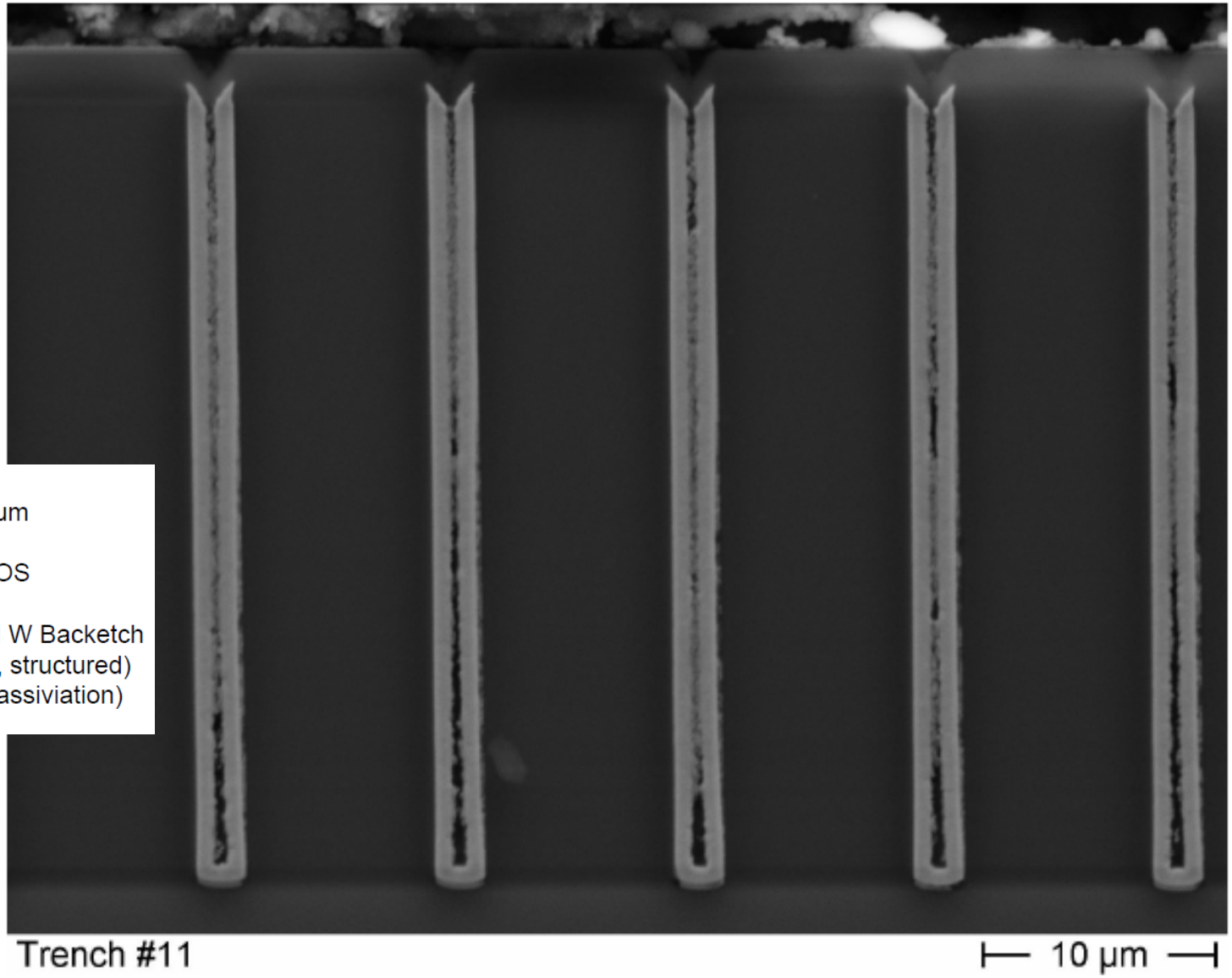


Bonding to handling substrate, thinning to 50 μm

Exposure of W in TSV and Alu spattering for creation of pads on the back-side

Through Silicon Vias processing

Fraunhofer EMFT



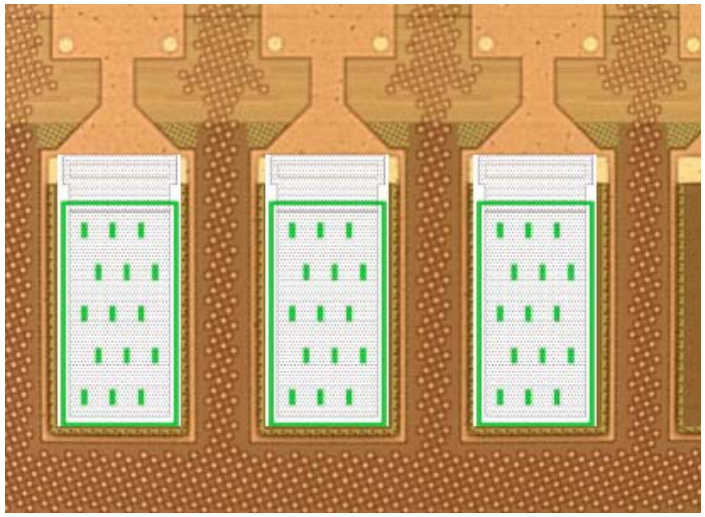
ICV-Dimensions:
3 µm x 10 µm x 50 µm

300 nm SACVD TEOS
20 nm TiN CVD
900 nm W CVD und W Backetch
800 nm M1 (AlSiCu, structured)
850 nm PN/POX (Passiviation)

Courtesy of R. Wieland, EMFT

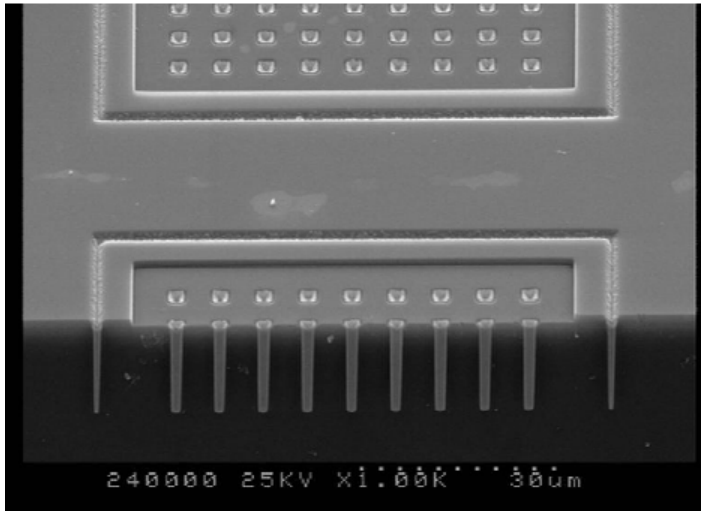
TSV in the FE-I3 chips

Fraunhofer EMFT TSV



➢ First etching trials on dummy wafer ✓

- Performed in the un-thinned FE-I3 chips of one designated test-wafer
- Etched to a depth of ~ 60 μm
- Optimize the trench width to obtain the same depth as in the TSV



➢ Process plan of the hot FE-I3 wafer

- Local planarisation of the fan-out pads by depositing and etching of SACVD-Oxide ✓
- Perform via etching and filling in the hot FE-I3 wafer
- Connect the readout chip with SLID to the hot sensor wafers

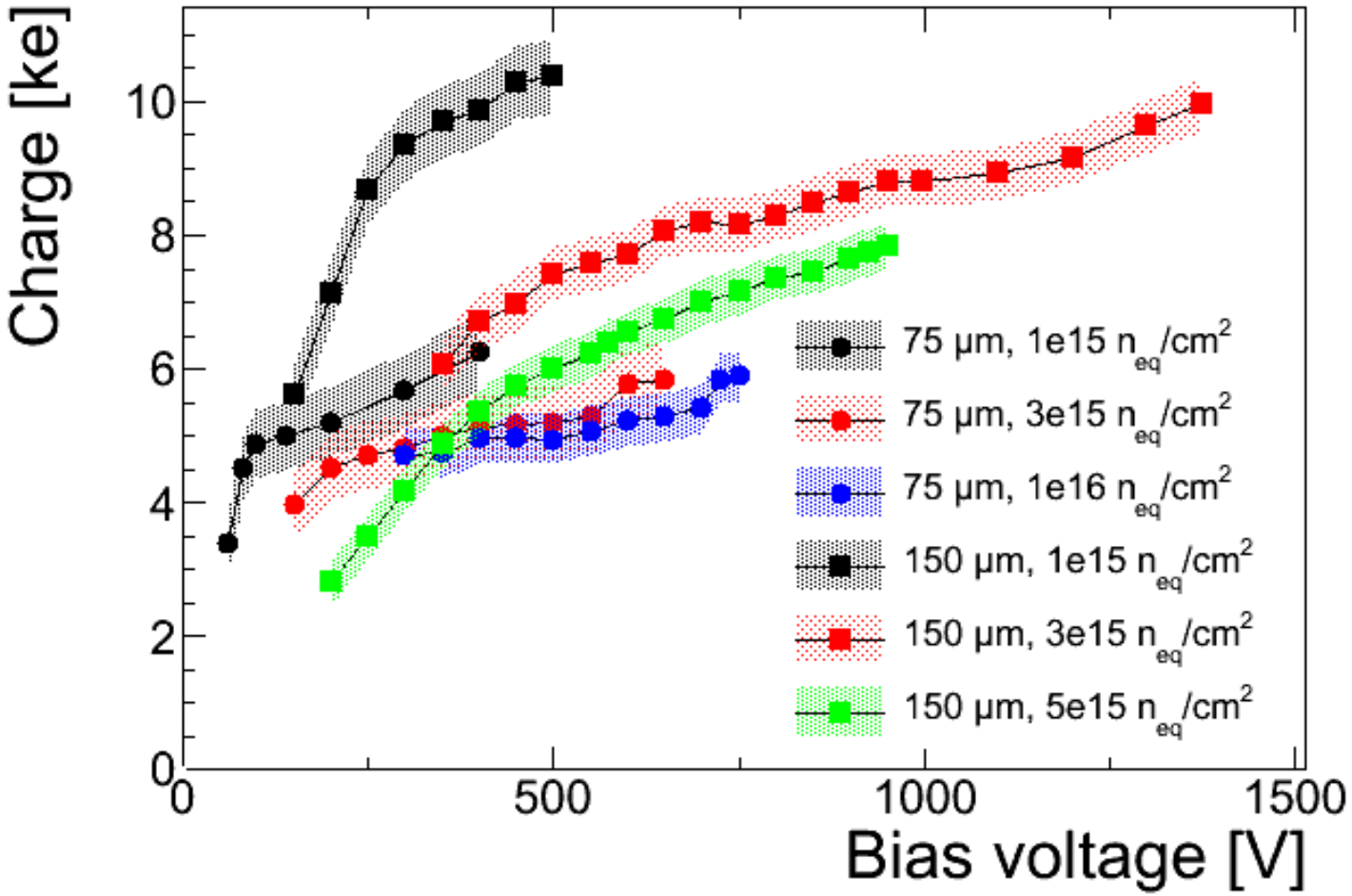
Summary and Outlook

- FE-I3 modules functional after SLID Interconnection, with extremely good performance (low noise, threshold dispersion, charge collection) before and after irradiation
- SLID withstands thermal cycling
- Challenging chip alignment on the handle wafer
- Systematic increase of not connected channels for a fraction the modules close to the wafer center→ due to the BCB contact opening, not related to the interconnection technology

Plans

- Optimize pick and place of the chips on handle wafer with new machines
- Full SLID assembly of sensors and FE-I3 chips with TSV
- Test the TSV approach on new ATLAS FE-I4 chip

Back-up Slides

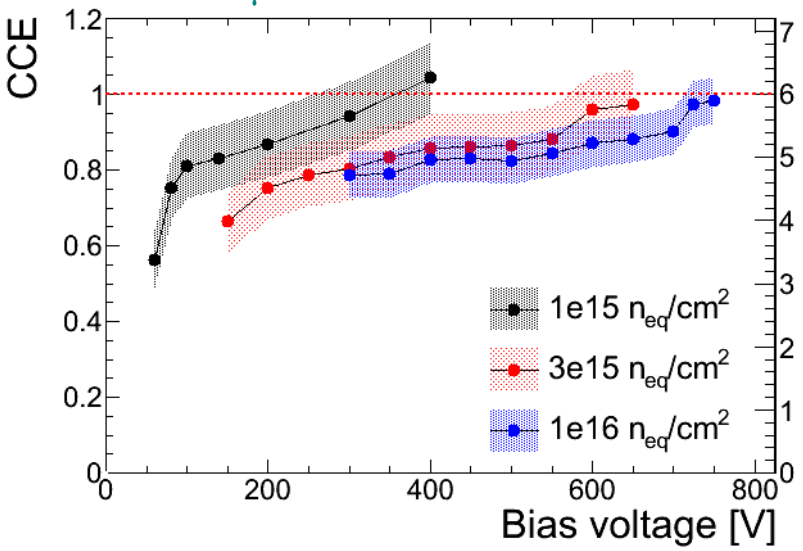

Charge [ke]
0
2
4
6
8
10
0
500
1000
1500
Bias voltage [V]
75 μm, 1e15 n_eq/cm²
75 μm, 3e15 n_eq/cm²
75 μm, 1e16 n_eq/cm²
150 μm, 1e15 n_eq/cm²
150 μm, 3e15 n_eq/cm²
150 μm, 5e15 n_eq/cm²

Thin pixels for the ATLAS pixel Upgrade

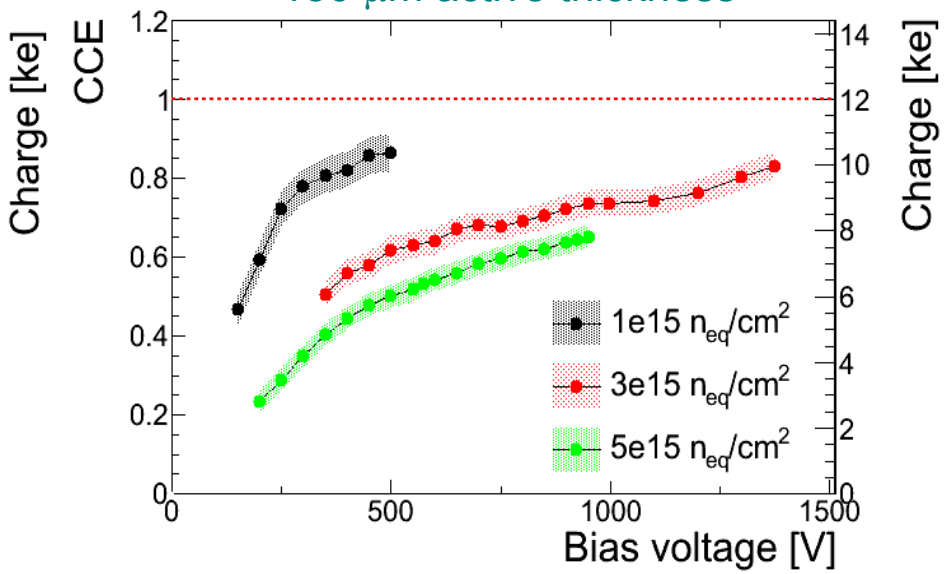
- ATLAS pixel system for the Phase 2 Upgrade: In the inner layers radiation doses of 1-2x10^{16} n_{eq}/cm^2 are foreseen
- Higher electric fields in thinner devices at equal V_{bias} : at HL-LHC fluences higher CCE is expected (larger drift velocity, charge multiplication)
- Minimize material and multiple scattering

Charge collection efficiency measured with thin p-type strip sensors produced by MPP-HLL – Alibava read-out system

75 μm active thickness



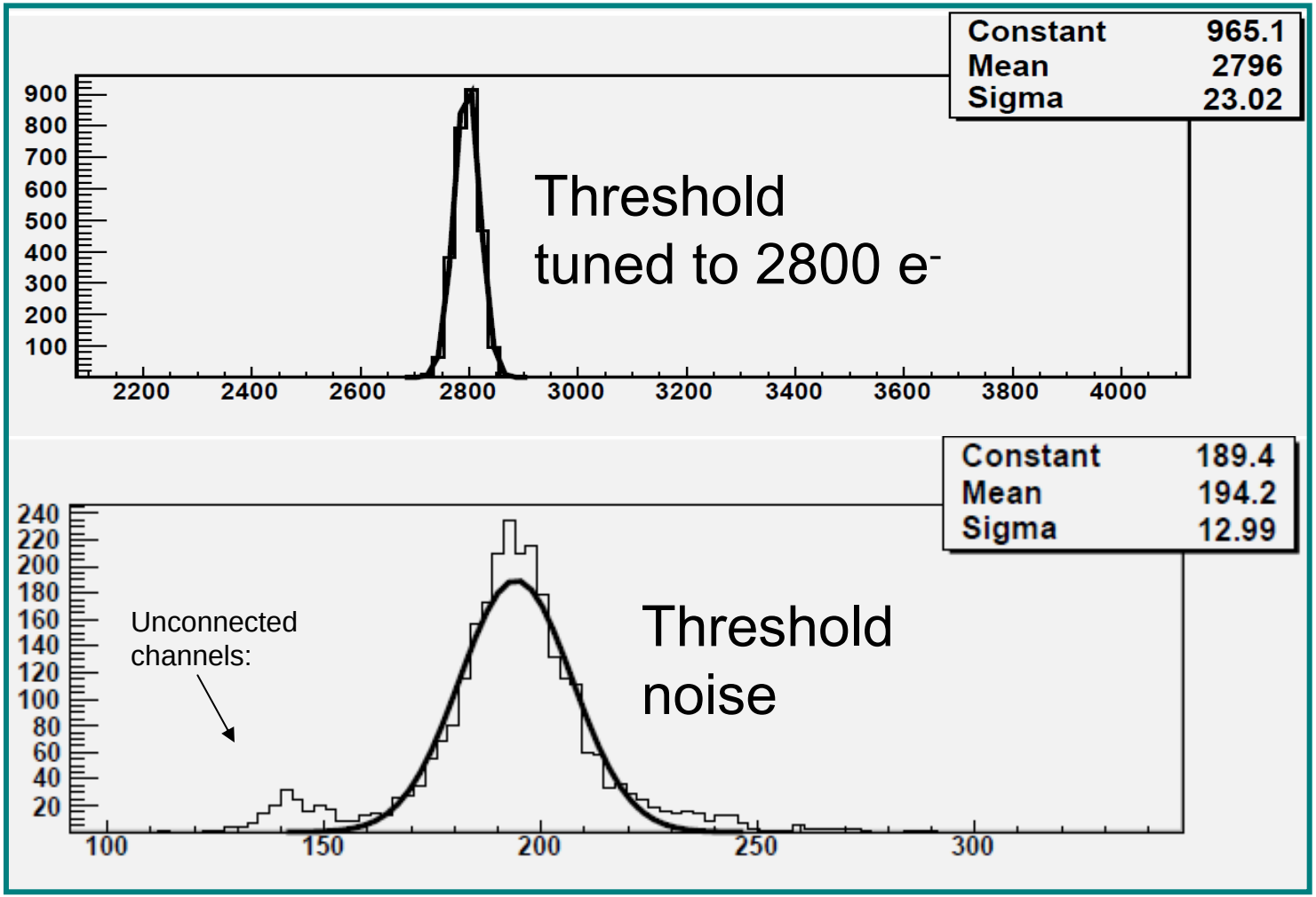
150 μm active thickness



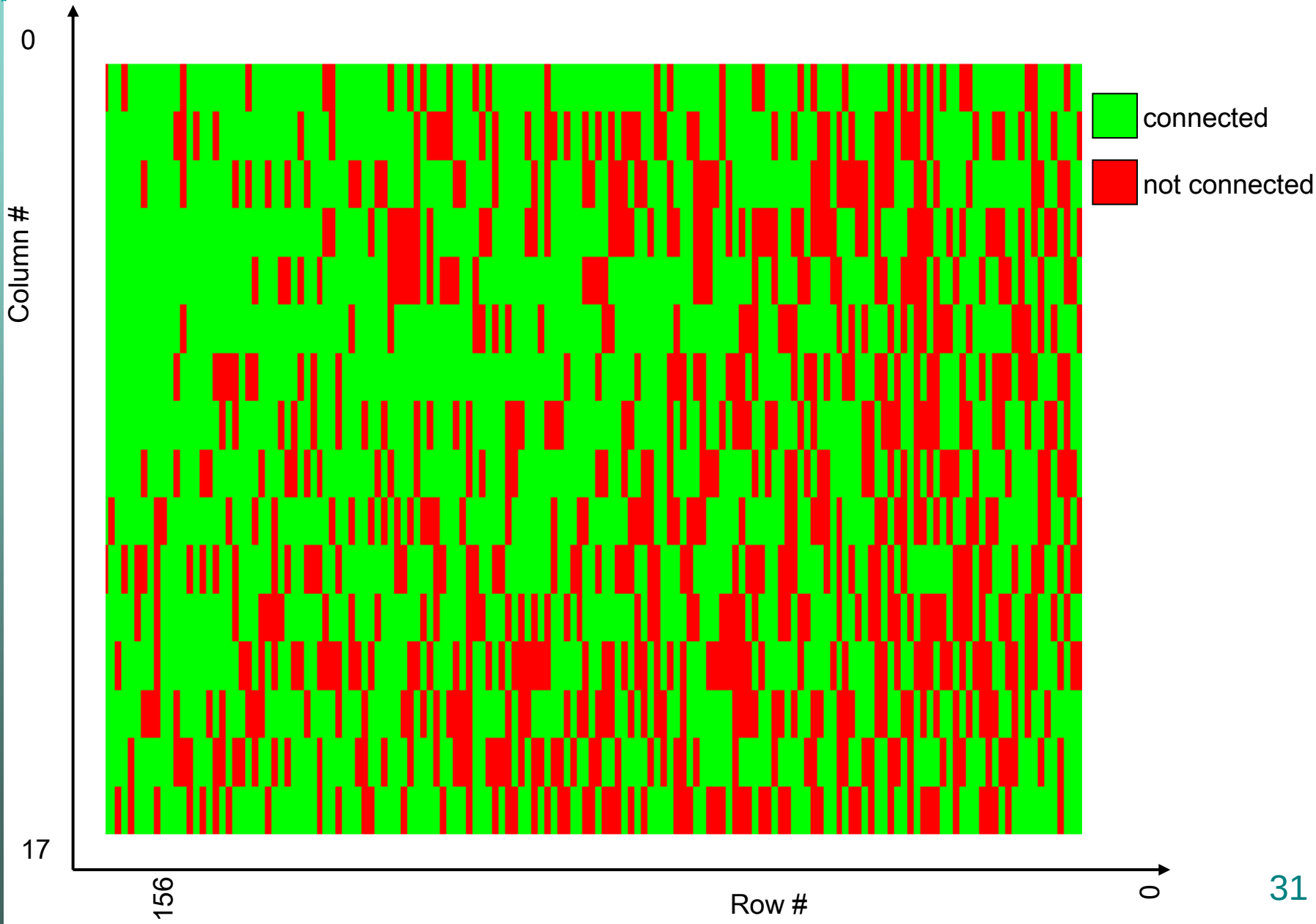
A. Macchiolo et al. http://dx.doi.org/10.1016/j.nima.2010.11.163

SLID Module 9: chip tuning

- Pixel with lower noise are an indication of unconnected channels

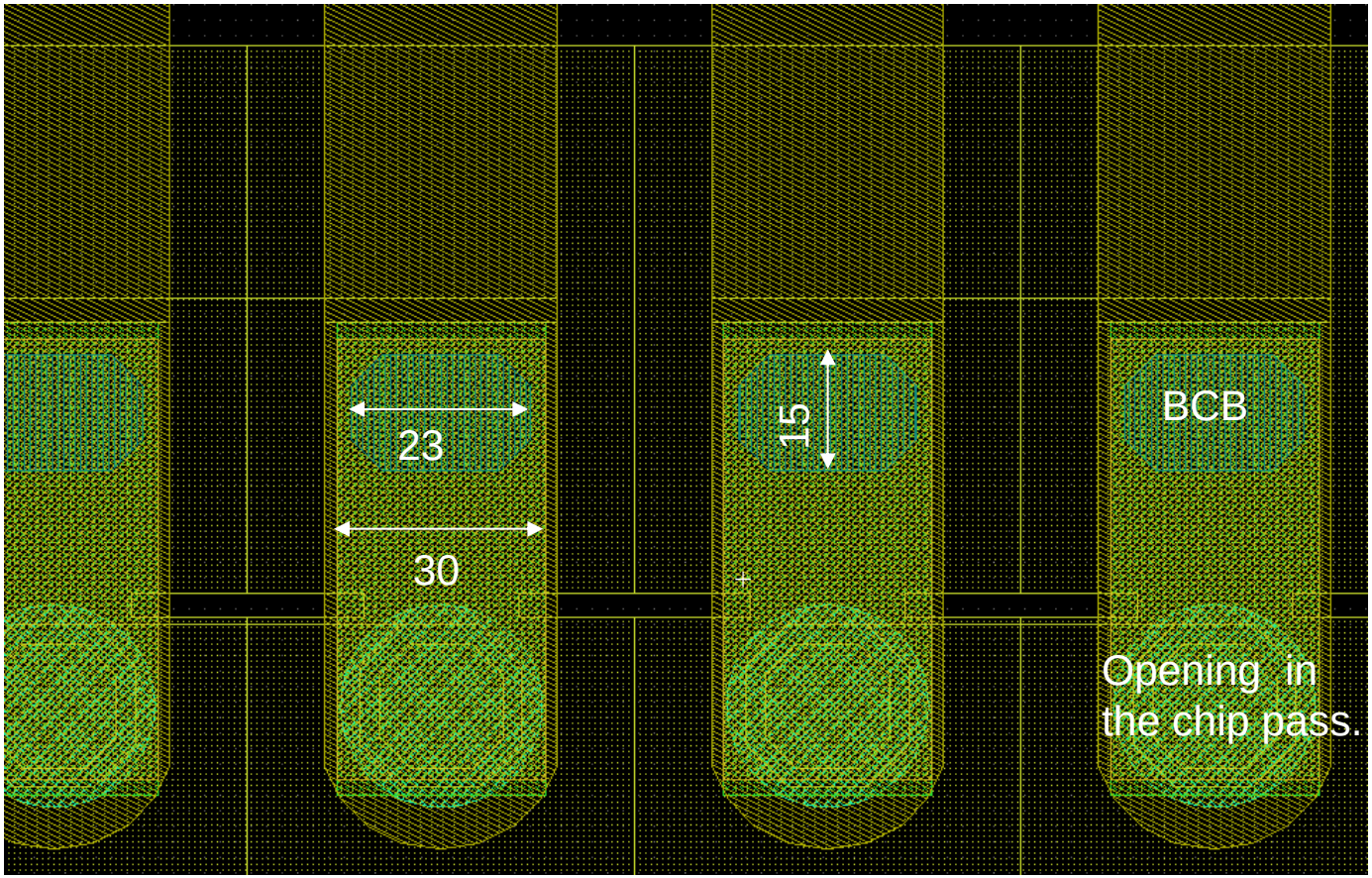


Connection map of SLID 7 module



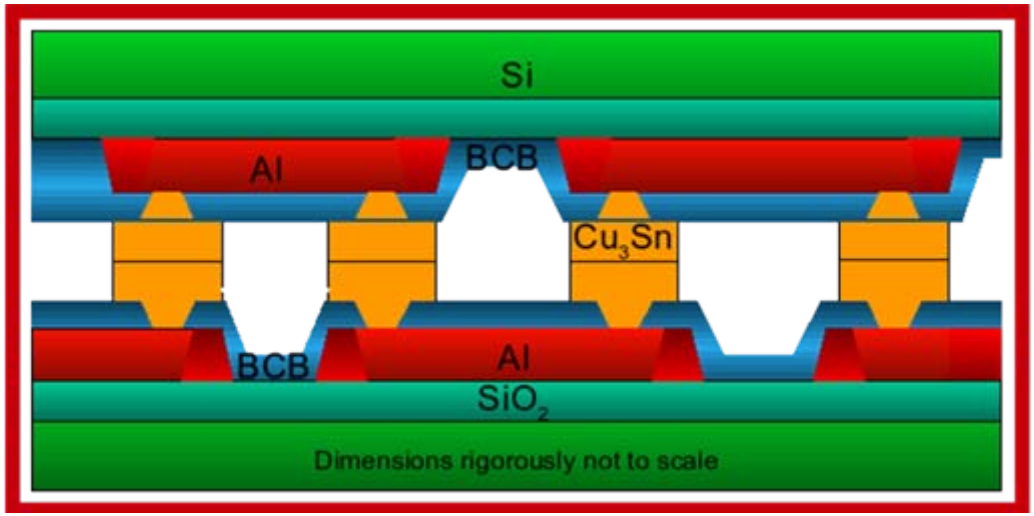
Causes of SLID inefficiency – BCB openings

- BCB passivation not completely open



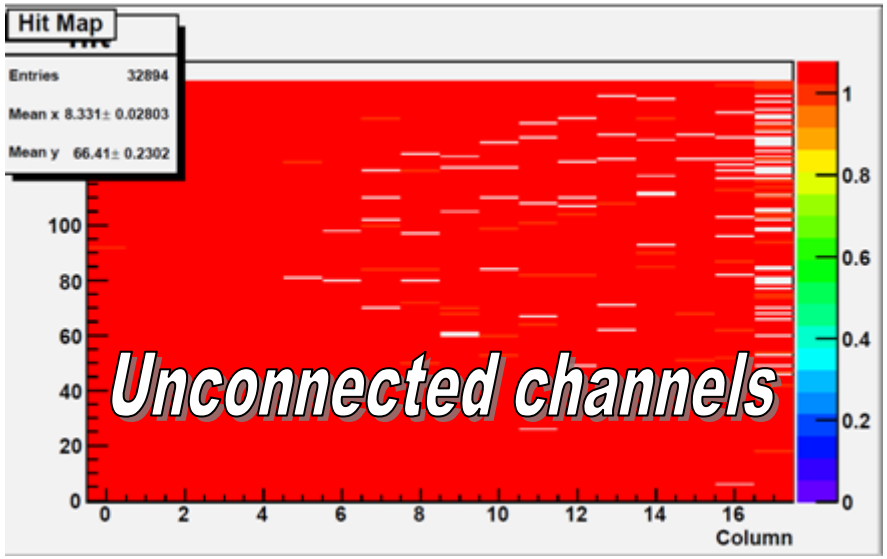
New daisy chain production for SLID testing

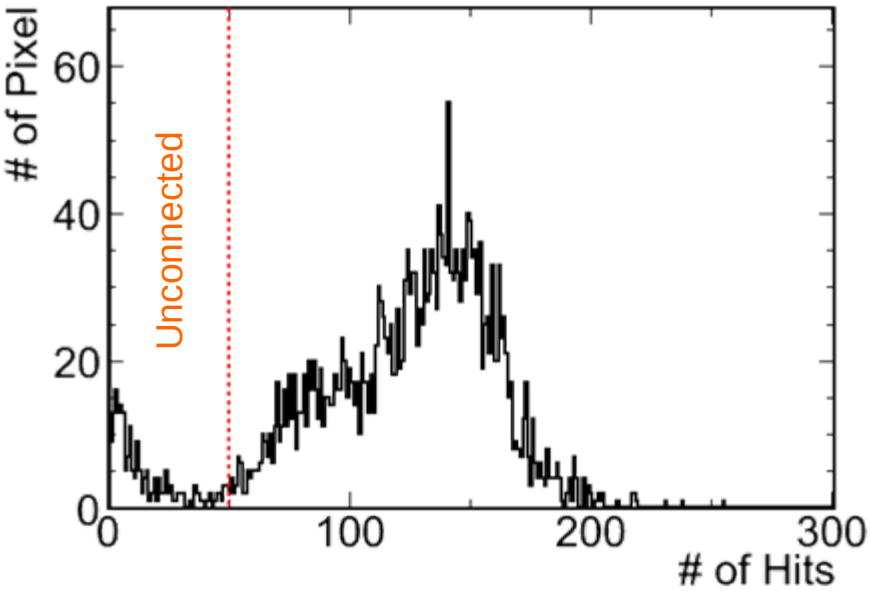
- FE-I4 geometry, daisy chains with 26800 pads each
- Arranged in the most regular pattern possible
- Test of the placement on the handle wafer with new flip-chipping machine at EMFT
- SLID efficiency with measurements of the electrical continuity



- EMFT can do the copper electroplating in house, tin will be available in October (subcontracted to IZM Berlin in the past).

SLID Module 9: Charge Collection





- Number of unconnected channels ~ 6%
- The module is fully functional except for the fraction of disconnected channel
- Similar results for SLID8-SLID7-SLID6 with an increasing number of unconnected channels.