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SLID-ICV interconnection technology for the ATLAS pixel upgrade at SLHC

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We will report on the characterization of pixel modules composed of 75 microns thick n-in-p sensors and ATLAS FE-I3 chips, interconnected via the SLID (Solid Liquid Inter-Diffusion) technology. This technique, developed at Fraunhofer-EMFT, is employed as an alternative to the bump-bonding process. These modules have been designed as a demonstration of a very compact detector to be employed in the future ATLAS pixel upgrades, making use of vertical integration technologies. This module concept also envisages Inter-Chip-Vias (ICV)to extract the signals from the backside of the chips, thereby achieving a higher fraction of active area with respect to the present pixel module design. In the case of the demonstrator module ICVs are etched into the original wire bonding pads of the FE-I3 chip. In the modules with ICVs the FE-I3 chips will be thinned down to 50 um. The status of the ICV preparation will be presented.

Summary 500 words

Our R&D activity is focused on the development of a new detector for the upgrade of the ATLAS pixel system at SLHC, employing thin pixel sensors together with a novel vertical integration technology offered by the Fraunhofer Institute EMFT in Munich. It consists of the Solid-Liquid-InterDiffusion (SLID) interconnection, which is an alternative to the standard bump-bonding, and Inter Chip Vias (ICV) for routing the signal vertically through the readout chips. The SLID interconnection is characterized by a very thin eutectic Cu-Sn alloy, achieved through the deposition of 5 microns of Cu on both sides, and 3 microns of Sn on one side only. This technology allows for stacking of different layers of chips on top of the first one, without destroying the pre-existing bonds. We will report on the characterization of pixel modules composed of n-in-p pixel sensors with an active thickness of 75 microns, produced at the MPP Semiconductor Laboratory (HLL), interconnected with SLID to the ATLAS FE-I3 chips. The interconnection has been performed with a "chip to wafer" approach. These devices have been studied with the ATLAS USBPix read-out system, that allows for the determination of unconnected channels, noise distribution and charge collection efficiency.
In the second phase of our project, ICVs are going to be etched on the original wire bonding pads of the FE-I3 chip. The tungsten filled ICVs have a cross section of 3 um x10 um and are prepared by etching through all the dielectric layers and the silicon bulk, that must be thinned down to around 50 microns. The signal transport to the readout pads on the backside of the chips allows for four side buttable devices without the presently used cantilevers for wire bonding. The ICVs etching is performed at the wafer level. The FE-I3 chips will then be singularized and connected to the sensor wafer with SLID.
The status of the ICVs etching on the FE-I3 wafer will be presented.

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