# FATALIC, a wide dynamic range integrated circuit for the tilecal VFE Atlas upgrade

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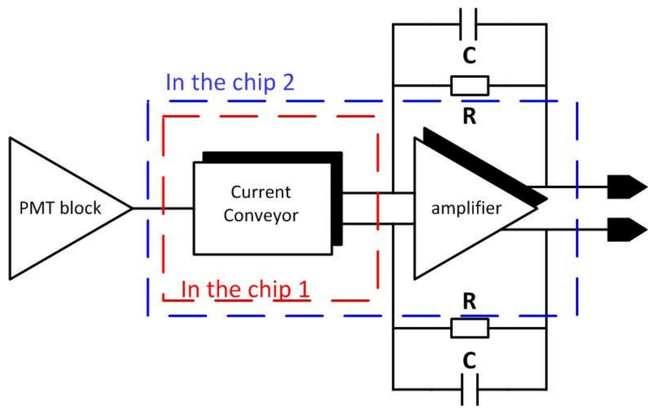
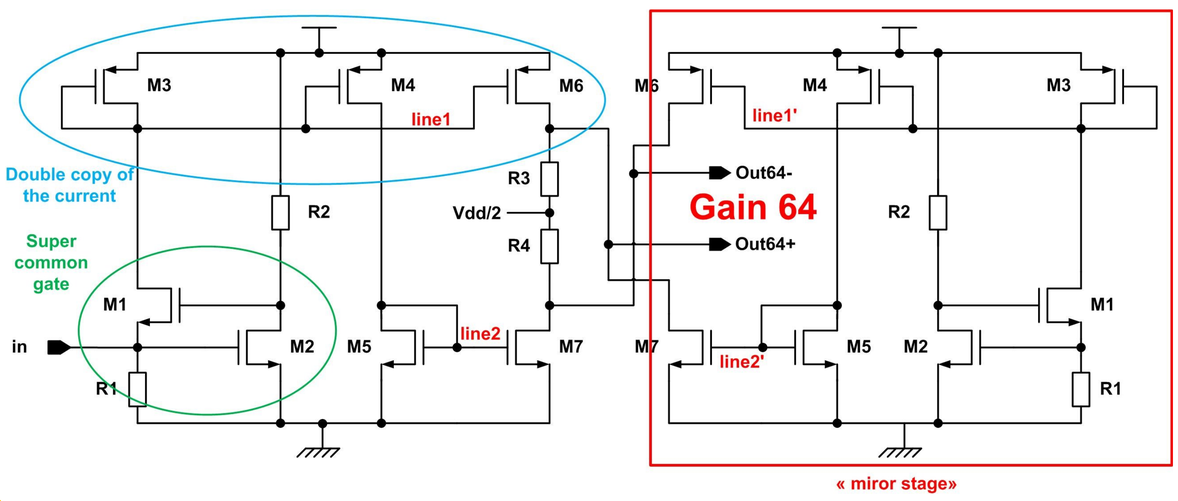
FATALIC 1 & 2

## Application :

Readout chanel for the Tile calorimeter of s-ATLAS experiment.



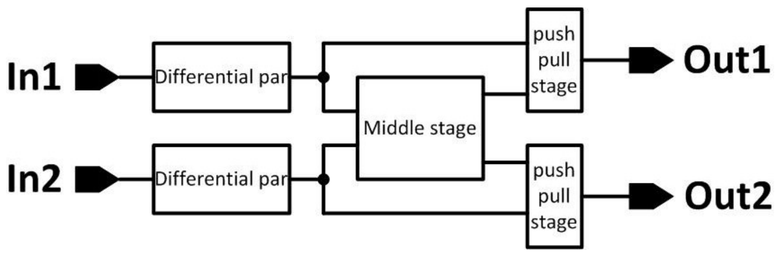

## Simplified schematic of the current conveyor (CC) :




## Specificities of the CC :

- « Super common gate » input
  → Input impedance ≈ 1 Ω.
- Double copy of the current allowing a differential output.
- Mirror stage for a suppress of the quiescent current.
- Three different output stages
  → three gains 64, 8 and 1 (normalized on 1V at the output), for an input current from 625 nA to 62,5 mA.
- Developed in **IBM CMOS 130 nm** technologie, voltage power of 1.6 V.

## Simplified schematic of the amplifier :

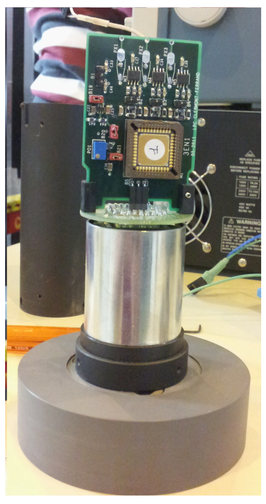


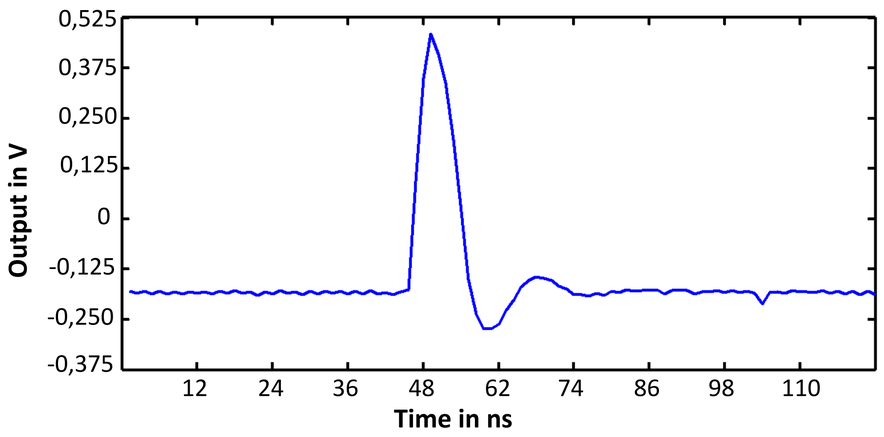

## Amplifier specifications :

- Amplifier without common mode feedback
- Open loop gain : 4400
- Phase Margin : 55°
- GBW : 260 MHz
- Noise : 60 µV rms
- Power consumption : 6,8 mW

## Test with the tileCal spare at Cern :

- Test with cosmic ray for Fatalic2

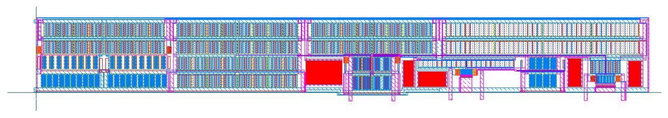





Output of the chip (channel gain 64) for a cosmic ray

## Dimensions :

- Chip 1 : 120 µm × 995 µm
- Chip 2 : 445 µm × 760 µm



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