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FATALIC, a wide dynamic range integrated circuit for the tilecal VFE Atlas upgrade

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The ATLAS upgrade will require more efficient electronics to fulfil the new performances expected by the experiment. Concerning the readout electronics of the Tile Calorimeter, the replacement of the 3in1 board by an integrated circuit is under study. The proposed circuit is composed of a multi-gain current conveyor, followed by shapers, an integrator for the calibration and an analog-to-digital converter. This solution presents better performances, concerning the noise, and the power consumption. Two prototype chips have been submitted using the IBM 130nm CMOS technology: one with a three gains current conveyor, another with an enhanced current conveyor associated with shapers.

Summary 500 words

The 3in1 readout electronic board of the ATLAS's Tile Calorimeter (TileCal) had been developed in the early 2000's. During the last ten years the development of ASICs has become more accessible, allowing integration of complex circuit in a single chip. It is why a development of a readout chip circuit dedicated to the upgrade of the TileCal of Atlas is in progress. This development will give an evaluation of the benefit induced by an ASIC solution.
The input amplifying stage is the key element of the readout electronics to be designed, because of the 17-bits (from 24 fC to 12 000 pC) dynamic range of the signal delivered by the PMT. In order to cover this dynamic range, an architecture in current has been preferred compare to a voltage one. The use of a current driven design presents major advantages: it allows to handle the whole dynamic range in the first stage, and to provide as many copy of the detector signal as needed for the different gain and functions (shaping or integrating).

The proposed readout is composed of a multi gain current conveyor (CC) followed by a shaper in order to improve signal-to-noise ratio. The readout electronics is completed with a 10 or 12 bits ADC with a sampling rate between 40 MS/s and 100 MS/s (final sampling rate and resolution are still in discussion). In parallel the CC is connected to an integrating stage for the calibration of the TileCal, a 10 bits ADC with a low sampling rate (approximately few hundred of kS/s) follows the integrator. The passive elements of the readout (such as resistors and capacitors for both the shaping and the integrating stages) will not be integrated in the design in order to configure precisely the different time constants.
A first circuit has been submitted in the 130 nm IBM CMOS technology. It is composed of a CC with three different gains (1, 8, 64) in order to cover the whole dynamic of the signal of the PMT. The circuit presents a small input impedance (about 1 Ohm), a differential output, and a quiescent current of 1 mA. A second chip including an optimized version of the CC associated with two injectors at the input and a shaper at the output has been submitted in a second time using the same technology. The main characteristics of the amplifier used for the shaping are:
- Open loop gain of 4400
- Phase margin of 55°
- Gain bandwidth product of 260 MHz
- Noise of 60 µV rms
- Power consumption of 6.8 mW

The next step in the project will be the design of the integrator required for the calibrations technics (the Cesium source and the laser beam).

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