Contribution ID: **51** Type: **Oral**

Development of low power Phase-Locked Loop (PLL) and PLL-based serial transceiver

Tuesday, 27 September 2011 14:50 (25 minutes)

The design and measurements results of low power Phase-Locked Loop (PLL) prototype for applications in particle physics detectors readout systems are presented. The PLL is designed and fabricated in 0.35˜μm CMOS technology. First measurements show that the ASIC is fully functional and generates clock in the frequency range 380MHz-1.1GHz. The PLL power consumption at 1˜GHz is about 4.5 mW. As one of main goals a transceiver comprising of PLL-based transmitter and receiver with PLL-based clock and data recovery circuit was designed, fabricated and tested. Proper functionality of the transmitter and receiver was verified in the frequency range 650MHz-950MHz.

Summary 500 words

In the modern and future detector systems of particle physics experiments, the data serialization and subsequent transmission with highest possible rate and lowest power becomes increasingly important, particularly in the context of continuously growing number and density of readout channels. The serialization and data transmision aspects are currently under study for the luminosity detector at the
future linear colliders (ILC/CLIC). Since the readout architecture of this detector comprises an ADC in each channel the data serialization from multichannel ADC need to be efficiently implemented. In a next step a fast power-efficient serial data transmission out of the detector is required.

In this work we first discuss the development of the core block for serialization and data transmission i.e. the PLL. We have designed two PLL prototypes. The design and performance of the second one, optimized for highest clock frequency and low power consumption, is discussed in detail. The first prototype was directly integrated into the prototype transceiver, comprising of a transmitter and receiver, for fast serial data transmission. In the second part of this work we discuss the design and results of measurements performed on the transceiver prototype.

A typical second order Phase-Locked Loop architecture was choosen for
the PLL design. It contains a Phase and Frequency Detector (PFD), a Charge
Pump (CP), a Low Pass Filter (LPF) and a Voltage Controlled Oscillator (VCO). The “current starved” inverters were used in the VCO design. To obtain the highest frequency, the good stability and the lowest power, a fixed divison factor equal 32 was used in the PLL feedback loop.
The full circuit was designed, simulated and fabricated in 0.35˜μm CMOS technology. The PLL layout occupies 160˜μm x 140˜μm.
The measurements of fabricated ASIC showed that PLL works in wide
frequency range, from 380˜MHz up to 1.1˜GHz at default 3.3˜V power supply.
The circuit functionality was also verified for lower supply voltages down to 2.1˜V. With decreasing supply voltage the maximum PLL output frequency was also continuously decreasing down to about 600˜MHz. With power supply increased to 3.5˜V the maximum PLL frequency increased to 1.2˜GHz.
For the default 3.3˜V power supply and at 1˜GHz PLL clock the measured power consumption was about 4.5˜mW.
The power consumption scales linearly with both, PLL clock frequency and power supply voltage.

The first version of PLL was used to generate high frequency clocks used
in data transmission/reception circuits of fast serial transceiver designed and fabricated in 0.35˜μm AMS technology. The transmitter circuit contains a parallel synchronous to serial asynchronous data converter and a phase-locked loop (PLL) block for clock generation. The
receiver circuit contains a clock and data recovery circuit (CDR) which
provides clock synchronization (using data slopes) and a serial to
parallel data conversion. Measurements showed full transmitter and receiver functionality and efficient data transmission between them was verified in the frequency range 650˜MHz-950˜MHz.
The detailed characterization of the transceiver performance is in progress.

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Session Classification: A2 - ASICs

Track Classification: ASICs