GEM400: A Front-End Readout Chip Based on Capacitor-Switch Array For Pixel-based GEM Detector

Li Huaishen, Jiang Xiaoshan, Liu Gang, Wang Na, Sheng Huayi, Zhuang Baoan, Zhao Jingwei
Institute of High Energy Physics, Chinese Academy of Sciences, P. R. China

Introduction

Gas Electron Multiplier (GEM) is one of new position sensitive gas detector developed by CERN. Its basic component is the kapton foil coated with copper on double sides, and etched with high density of micro holes. In working condition, high voltage is applied between the two copper sides, the electrons can be avalanched inside the holes, leading the amplification of primary ionization. GEM detector has a lot of excellent performance, such as high counting rate, high space and time resolution, it shows potential applications in many fields.

The upgrade of Beijing Synchrotron Radiation Facility (BSRF) need two-dimensional position-sensitive detection equipment to improve the experimental performance. GEM detector, in particular, pixel-based GEM detector has good respects in the domain of synchrotron radiation and high energy physics experiments for its simple structure, superior performance and the flexible way of read-out.

For the read-out of larger scale pixel-based GEM detector, we proposed a circuit structure based on the capacitor switch array circuit, we did analyze and simulation of the circuit. Then, we designed the chip GEM400, a 400-channel ASIC based on capacitor switch array circuit. The simulation results show that the chip can allow the maximum amount of input charge 70pC on the condition of 100pF external integrator capacitor. Besides, the chip has good channel consistency and better noise performance and lower consumption. We proposed a readout scheme for pixel-based GEM detector, this scheme is based on GEM400 chip and System-in-Package technology.

The GEM400 ASIC chip is built with Global Foundries 0.35um CMOS 2P4M process. The basic functional circuitry in this chip includes analog switch, analog buffer, voltage amplifier, bandgap and control logic block. Its layout takes 5mm x 5mm area.

Fig. 1: GEM kapton foil hole, the pitch is 140um

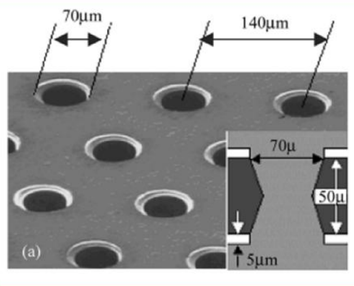


Fig. 2: Triple-GEM diagram

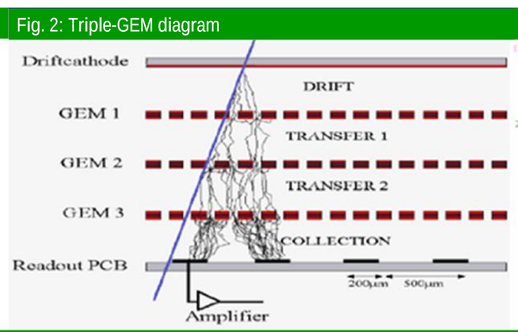
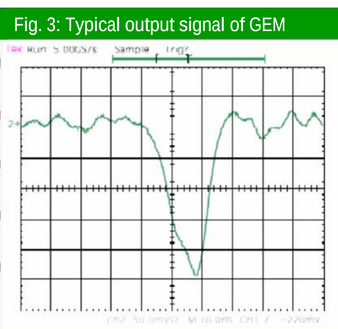


Fig. 3: Typical output signal of GEM



Signal Characteristic and detector parameter

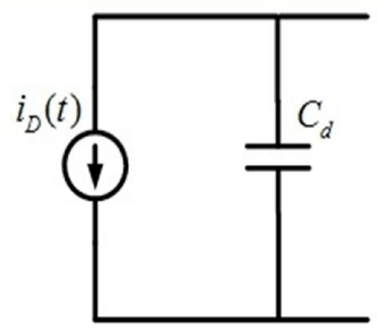
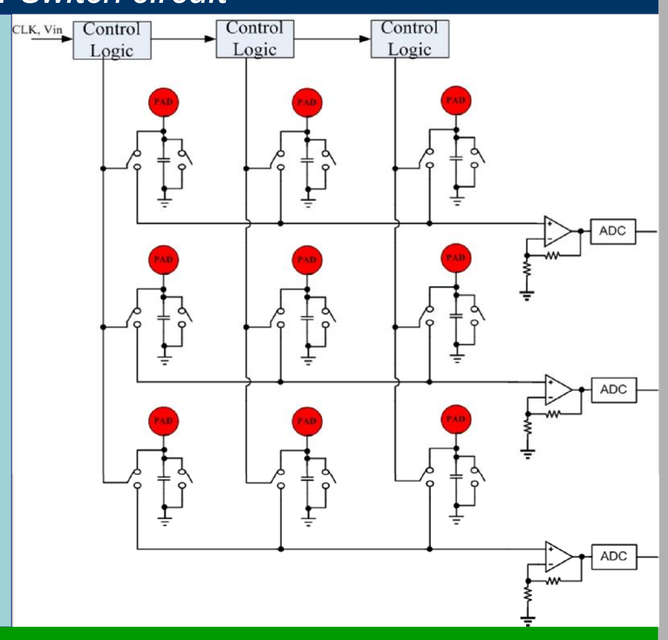


Fig. 4: Equivalent model of GEM detector. A current source and a capacitor is included, the capacitor Cd is about 10pF.

Class	Value
Total Rate	10,000,000Hz/s
Rate per channel	1,000,000Hz/s
Q per hit	30fc~300fc
Noise/channel	3~6fc
Signal Rising Edge	25ns~40ns
Signal Falling Edge	60ns~90ns

Capacitor Switch circuit

Fig. 5: Capacitor Switch Circuit. It is a diagram of 3x3 Pad array. There is only two analog switch and one integration capacitor, it is consume lower power, and the Pad is read-out line by line.
First, all the switches are open, and charge accumulated on the integration capacitor, then, switches of line1 are closed, the voltage on the int. capacitor of line1 is measured, after that, switches of line1 are open and line2 are closed, the voltage on the int. capacitor of line2 is measured……
Using the capacitor switch circuit, the readout system can be very simple.



Analyze of the capacitor switch circuit

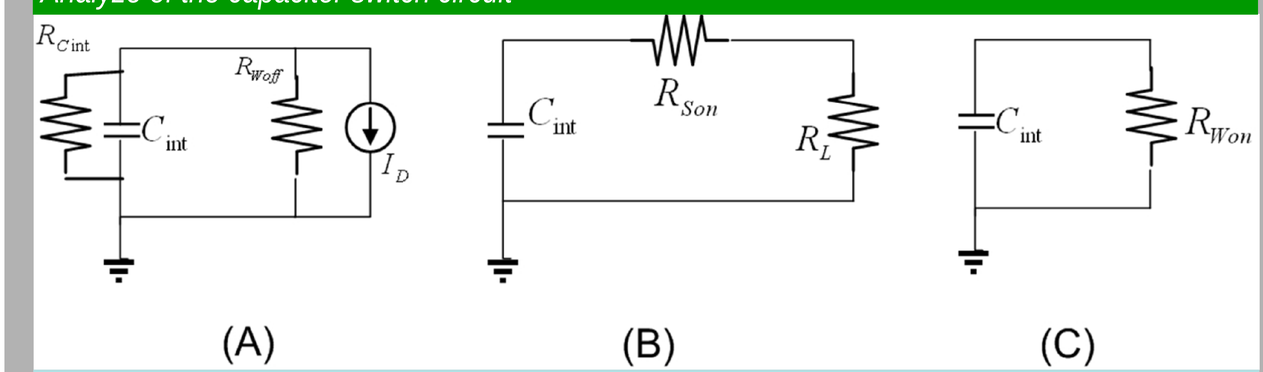


Fig. 6: Three working condition of the capacitor switch circuit.
Condition 1: Fig. 6(A), Integral status, the discharge switch and the gating switch are open, and charge accumulated on the int. capacitor.
Condition 2: Fig. 6(B), the discharge switch is open, the gating switch is closed, the voltage level of the int. capacitor is collected by the back-end circuit.
Condition 2: Fig. 6(C), the discharge switch is closed, the gating switch is open, the charge of the int. capacitor is discharged.

The read-out board structure of the Pad array

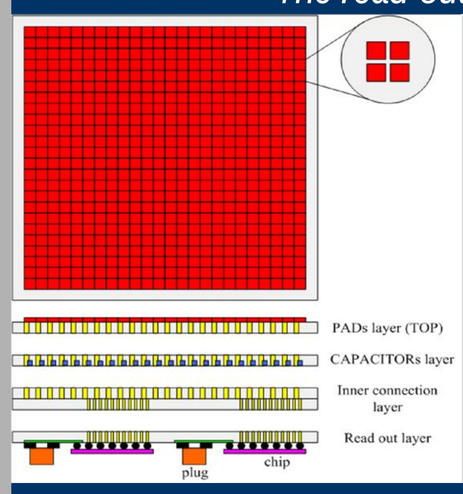


Fig. 7: The Read-out board structure of the Pad array
For this capacitor switch read-out scheme, the int. capacitor must be large enough, here we use 100pF capacitor. This CAP cannot be achieved in CMOS process, so we use external CAP as the int. CAP.
The CAP we choose has zero temperature coefficient, lower leakage current, higher insulation resistance, the CAP is embedded into the PCB board.
The GEM400 AISC is attached to the board through wire-bonding.
The pitch is 1mm

GEM400 ASIC Design

Fig. 8: GEM400 chip circuit
Process: GF 0.35um 2P4M baseline process
Channels: 400
Int. CAP: 100pF
Gating time per ch: 200ns
Cycle time: 80us
Discharge time: 400ns
Leakage: <10pA
Chip Area: 5mm x 5mm

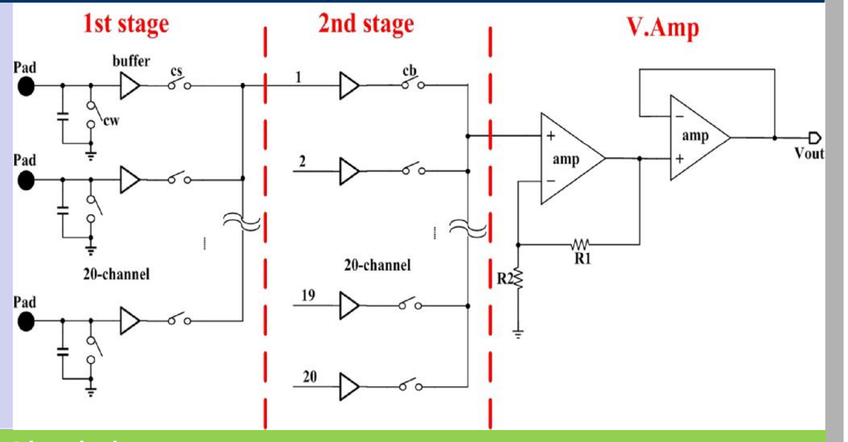
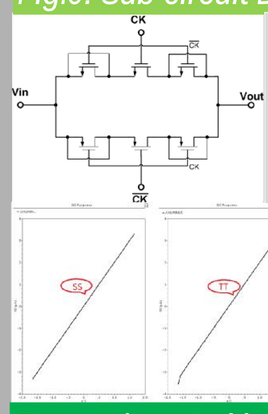
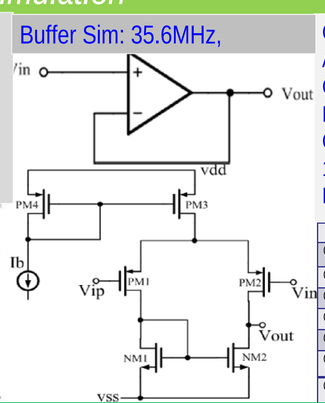


Fig.9: Sub-circuit Design and Simulation

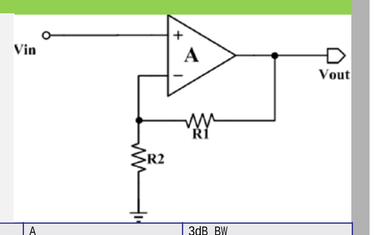


Discharge Switch Sim:
Ron: 150 Ω
Leakage current: <3pA

Buffer Sim: 35.6MHz,



OPA Sim:
AoI: 88.7dB
GBW: 79MHz
PM: 60°
Output swing: -1.451~1.445V
Power: 3mW



	A	3dB BW
Cload=1p	6.02dB	48.5MHz
Cload=2p	6.02dB	49.1MHz
Cload=4p	6.02dB	48.7MHz
Cload=8p	6.02dB	47.1MHz
Cload=16p	6.02dB	38.6MHz
Cload=32p	6.02dB	32.1MHz
Cload=64p	6.02dB	24.0MHz

Bgp and control logic sim

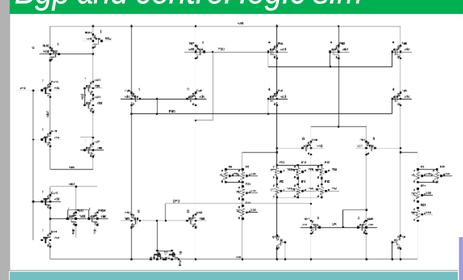
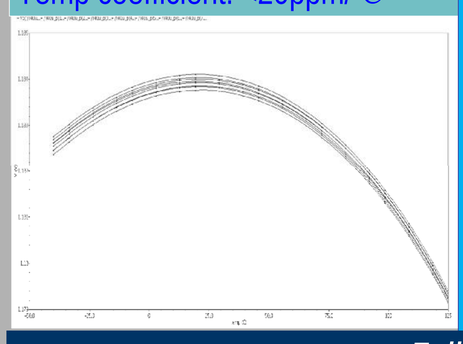
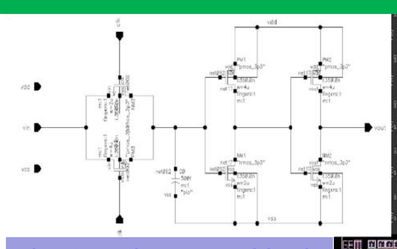


Fig. 10: Bandgap Sim:
Temp coefficient: <20ppm/℃





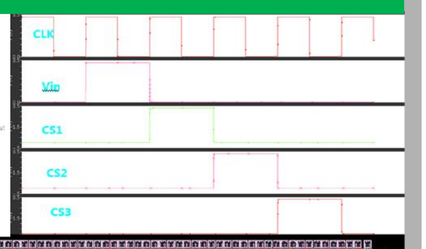
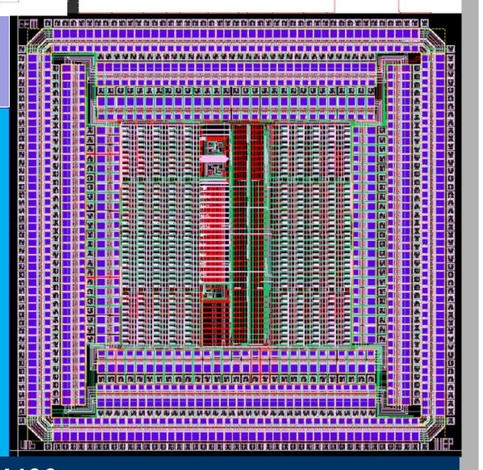


Fig. 11: The control logic and simulation result.

Fig. 12: Layout of chip GEM400, the chip has 432 pins.
Area: 5mm x 5mm
Power: 27.2mA x 3.3V
Power supply: Vdd=1.65, Vss=-1.65



Full Simulation of chip GEM400

In the design of GEM400 chip, we divide the chip into several blocks, design and simulate the single block first. When all the blocks are completed, we do full simulation of the chip.

Fig. 13: transient simulation

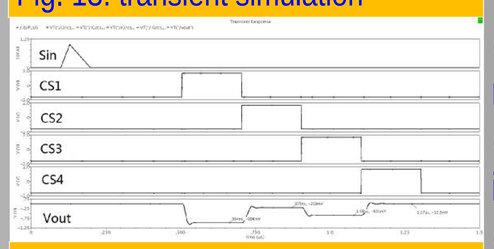


Fig. 13: Linear dynamic range sim. , the range is -0.7V~0.35V

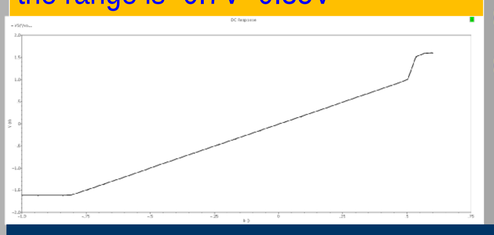
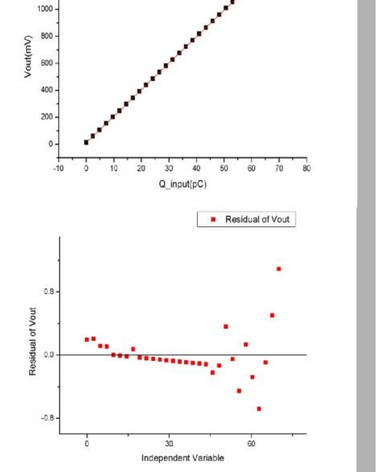


Fig. 14: Linear simulation
@ --Linear output voltage range:-1.388V~0V
@--Maximum equivalent input charge: 70pC
@--Output offset: -12.26mV
@ --INL: <0.1%
@ --Gain: 19.6406mV/pC



Conclusion

(1)Circuit performance will meet to our requirements based on our designs.
(2)Capacitor Switch circuit is suitable to pixel-based GEM readout, it can deal with high rate X-ray, and get good position resolution, it shows potential applications in many fields.
(3)More challenging work need to be done on the ASIC design for pixel-based GEM detector.

lihs@ihep.ac.cn