Contribution ID: **67** Type: **Poster**

AGET-SED : A 128-Channel Complete Data Acquisition system for solid state and gaseous detector

Thursday, 29 September 2011 16:00 (2h 30m)

To prepare future experiment, we need to qualify new solid state detectors and gaseous TPC. From T2K experiment and GET project, we develop a small board constituted of two 64 AGET asic, a 4-channel pipeline adc and a smart commercial board called "AVNET minimodule"to sequence the acquisition and send data in TCP/IP mode through the Ethernet network. The size of the board is 15 cm x 8 cm. Thanks to its small size, the board can be plugged close to the detector channels in vacuum or in gaseous environment. The paper presents the architecture of the system, performances and test result on micromegas readout plane, beam tracking detector and double sided stripped silicon detectors.

Summary 500 words

With a derivative of the AFTER[1] asic development, we extended our work to build a prototype of the AGET-SED based on the AFTER circuit. We were able in test its performance with beam experiment at GANIL to show that data processing was able to characterize gaseous detectors for beam tracking. Despite the fact that it satisfied data processing requirement, the prototype has several inconvenient. It is triggered externally by another DAQ system. So it is very difficult to use it with solid state detector. The data compression was not enough to reach sufficient data rate for validating completely the performances of detectors. As consequences, AFTER was replaced by the evolved version AGET asic circuit, developed within the GET collaboration. Further the embedded software was enhanced through a choice of performing architecture. It is the AGET-SED system.

AGET-SED specifications cover a relatively wide charge dynamic ranges and several level numeric trigger for pulse shape recording with event rate of up to 1 kHz. The board layout includes two 64-channel AGETs and ADCs together with built-in synchronization and inspection features controlled by the "avnet minimodule" . This minimodule consists of SDRAM, Virtex-4 FX12 FPGA, 10/100/1000 base Temac interface for Ethernet communication. The software is based on ICE-E middleware open source framework running on VxWorks operating system. .

Each AGET channel includes a test pulse input, a charge sensitive preamplifier, a shaper, a leading edge discriminator and a 512-cell analog memory, SCA. The gain, polarity, shaping time and threshold can be programmed individually for each channel by slow-control, SC. Use of external preamplifier and shaper instead of the internal ones is integrated. Shaped signals are continuously sampled (1-100Mhz) and written onto the circular SCA, which is read by an external 12 bits 20MHz ADC under request. The readout of the SCA can be selective (programmable time window, and selected on only hit channels). Outside this readout phase the same ADC also codes the multiplicity information constructed from the discriminator outputs to give trigger information.

First results from DSSD detector, TPC and beam tracking gaseous detector will be presented during the conference.

References

[1]AFTER, an ASIC for the Readout of the large T2K time projection, P. Baron,E. Delagnes, D. Calvet, X. de la Broise, A. Delbart, F. Druillole, J-L Fallou, E. Mazzucato, E. Monmarthe, F. Pierre, A. Sarrat, E. Zonca, M. Zito. IEEE Transaction on Nuclear Science, Vol. 55, N°3, June 2008, 1744-1752.

Shebli Anvar1 , Pascal Baron1, Denis Calvet1, Thomas Chaminade1, Joël Chavas1 ,Frederic Druillole1, Estelle Monmarthe1, E. Pollacco2.
1 CEA Saclay, IRFU/SEDI , 2 CEA Saclay, IRFU/SPHN

Primary author: Mr DRUILLOLE, Frédéric (CEA Saclay)

Presenter: Mr DRUILLOLE, Frédéric (CEA Saclay)

Session Classification: Posters

Track Classification: Systems