The Electronics System of the ALFA Forward Detector for Luminosity Measurements in ATLAS

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ALFA : Absolute Luminosity Measurement

Each “RP” is a 20x20mm mini tracker made of 10 planes of staggered scintillating fibers in U and V directions, plus 2 scintillating plates covering the tracking area for producing trigger signals.

Two small trackers symmetrically placed around the proton beam, the detector to beam distance can be as low as 1.5mm. Measure the elastic beam scattering at very low distance of the beam.

One “UP”

One “DOWN”

Two small trackers symmetrically placed around the proton beam, the detector to beam distance can be as low as 1.5mm. Measure the elastic beam scattering at very low distance of the beam.
ALFA R/O electronics

In alcove: LV power supplies

RR13 alcove

USA15 counting room

USA15:
- HV units
- DCS control & monitor
- ROD
- LV PFC and control
- CTP

In alcove: LV power supplies

RR17 alcove

250m + through tunnel & galleries

Each station (A, B):
- 2 pots (up and down)
- 2 readout systems (PMF + Motherboard)
- 1 (main) Patch Box
- 2 HV dispatchers

For A&B:
- 1 optolink dispatcher

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ALFA R/O electronics

In alcove: LV power supplies

RR13/17 alcove

LV voltages

Patch Box B

Patch Box A

380V DC

Maraton Control

Control & Monitoring (DCS)

USA15 counting room

USA15: HV units
DCS control & monitor
ROD
LV PFC and control
CTP

Connections

Source/dest.

<table>
<thead>
<tr>
<th>Connections</th>
<th>Source/dest.</th>
</tr>
</thead>
<tbody>
<tr>
<td>LV Power</td>
<td>Local alcoves</td>
</tr>
<tr>
<td>TTC</td>
<td>USA15, fiber</td>
</tr>
<tr>
<td>Data (Read)</td>
<td>USA15, fiber</td>
</tr>
<tr>
<td>Control &amp; Monitoring</td>
<td>USA15, CAN bus</td>
</tr>
<tr>
<td>HV</td>
<td>USA15, electrical</td>
</tr>
</tbody>
</table>
ALFA R/O electronics

TRIGGER SIGNALS

USA15:
- HV units
- DCS control & monitor
- ROD
- LV PFC and control
- CTP

Connections | Source/dest.
--- | ---
Main Trigger | Air core, USA15 (CTP)
OVLP Trigger | USA15, electrical
### ALFA R/O electronics

#### Track Data Flow

- **PMT readout**
- **L1 Buffer & serializer 40Mb/s**
- **Serializer 1.2Gb/s**
- **ROD**

#### Configuration Flow

- **PMT readout**
- **Registers**
- **SPI interface**
- **DCS**

#### Trigger Flow

- **PMT readout**
- **Mask/AND**
- **Line Drivers**
- **CTP, Trigger Logic**

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**FE structure**: PMF

**On Each Pot**: MAROC - ALFA-R - Motherboard - Tunnel - USA15

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ALFA R/O electronics

Tracking Data flow on each detector

Data Flow

PMT readout | L1 Buffer & serializer 40Mb/s

Trigger Latency

Buffer & Serializer

Serializer 1.2Gb/s

On Motherboard

Kapton cable

From PMT

A

D

MAROC2 ASIC
Fast Shaper
Per channel adjustable Gain
Variable Threshold

ALFA-R FPGA
Trigger Latency
Buffer & Ser. MAROC2 configuration

Trigger

ALFA-M FPGA
Buffer & Ser.
Data Format
ALFA-R Data Flow control
SPI interface

To USA15

FE structure: PMF (23x)

Amplifier
Discriminator

64 channels

23x

64 channels

23x
ALFA R/O electronics

• Aimed for compact, removable electronics
• Minimal cabling constraints (from USA to RP)
• FE Electronics centered around the MAROC2 ASIC developed by LAL/Orsay for MA-PMT readout systems
• Partial Radiation Hardness (Power supplies and regulation, ELMB, TTC GOL QPLL etc ...)

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Detector and Front-End Parts

3 stacked PCB mounted on the MAPAMT pins: HV distribution, signal distribution, active layer (pictures on the right)

Maroc side

ALFAR FPGA side
Detector View

- 10 tracking modules, 3 overlaps and 2 triggers
- 1460 fibres and trigger lightguide bundles to optical connectors
- 2 LED and 2 PT100 sensor
ALFA Electronics on each pot

23 PMFs:
5 rows
1460 readout channels

Connections | Source/dest.
---|---
LV Power | Local alcoves
TTC | USA15, fiber
Data (Read) | USA15, fiber
Control & Monitoring | USA15, CAN bus
Triggers | USA15, electrical

Targets:
Collects and serialize data from 23 PMFs
Long distance links to USA15 (no repeaters)
Independent control and monitor through ELMB
Removed from tunnel when not in use
Functions distributed in the front-end electronics

ALFA_T functions:
- Local Trigger Pattern
- Main Trigger Charge
- Trigger rate counter
- LED pulser

ALFA_R functions:
- Tracking Pattern
- Track Detector Charge measurement

ALFA_M functions:
- SYNC & SEND DATA
- Track Detector Charge measurement*
- SPI interface (PVSS control)

ELMB/PVSS functions:
- MAROC configuration
- Channel masking
- LED Pulse parameters
- Trigger pattern configuration
- Latency adjustment
- Monitoring

* : Special run, very low trigger rate, standalone ALFA, special data format
Motherboard Main Functionalities

- 23 PMFs for measurement with 64 pixels >> 64 bits of data for each PMF
- PMF passes its raw data serially to the ALFA-M controller
- ALFA M collects raw data with the same L1ID and then transmit it through a GOL link to the ROD

- System clocked at 40MHz, few KHz L1 rate
- 11A, 5V (with 23 PMFs)
Motherboard Details

Interface to Trigger Mezzanine

FPGA
ALTERA
EP3C40F780C6
N

Capability of track charge measurement (to measure charge collection degradation)
Trigger Mezzanine Functionalities

- 4 “LUCID” PMFs for Trigger charge measurement and time detection
- Triggers Outputs are programmable combination of Trigger inputs (2 main, 2 OVLP)
- Two programmable pulse generators for in-detector test LEDs

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Main1 Trigger
OVL1 Trigger
Main2 Trigger
OVL2 Trigger

Main Trigger PMF
OVL1 PMF
Main Trigger PMF
OVL2 PMF

Mezzanine

ALFA T FPGA

Drivers

Test LEDs (2)
Main Trigger (1)
OVL1 Trigger (2)

MB connector
MB connector

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Trigger Mezzanine Details

Capability of trigger charge measurement: the trigger charge is measured and transmitted at every L1, together with tracking data and the trigger pattern.

Interface to "LUCID" PMFs (LUND Devlpt.):
Two PMFs plugged on the mezzanine; two interface holding lemo inputs and attenuators on top of LUCID PMFs.

Interface to MB:
Two connectors to bring power and to interface with ALFA-R: clock, config bus, trigger pattern, qdc outputs; spare single ended and LVDS IOs.

FPGA
ALTERA EP3C25F256CN

QPLL (40MHz LVDS)
SPI Bus (from MB)
Trigger Pattern (LVDS @ 40 MHz)
Trigger Data (LVDS @ 40 MHz)
Spare IO (8)
Spare LVDS (3)

PMF Config
ADC
ADC

Trig1,2
Trig3,4

Main Trigger
Overlap 1
Overlap 2

NIM Drivers

LED Pulse
DAC

LED Driver

Air-core
OVL1
OVL2

LED1
LED2

Regulators

+7V (MB)
+5V (MB)
The Trigger mezzanine contains the circuits for:

- LED Pulsers (2 LEDs installed in each pot for light excitation)
- Trigger Logic (trigger signal can be a combination of the 4 trigger sources)
- Main Trigger charge measurements
- Triggers signal processed by the MAROC2 chip, mounted on the LUCID PMF
ALFA “Motherboard” implementation

Trigger Mezzanine

ELMB: control and monitoring

Power Conn.  GOL link  TTC Fiber  ELMB Conn.1  ELMB Conn.2  Temp Connector
Partial view of the kaptons cabling, PMF are located inside, HV connectors on the right trigger signals on the left. White wires are the internal HV lines.

PMT, PMF and kaptons are enclosed in a dark box, the motherboard carrying other elements (ELMB, trigger mezzanine) is vertical on the edge.
Electronics commissioning was performed on the 8 systems just before installation and repeated after installation.
Electronics commissioning

Electrical test stand: one charge signal injected in one channel. The method was used to verify the channel mapping for DAQ reconstruction.

LED test stand: one long distance LED (about 1m and light diffuser) is used to illuminate all channels. In this plot one PMF “row” is not operational, as well as a 3 other PMTs (HV off).
Internal LED pulser: light is passing through leaks in the optical connectors. More light at the center (where the LED is located). Test on one RP system after its installation in the tunnel.
Electronics commissioning

Internal LED pulser: ON LINE MONITORING

Top left figure: on-line hits display

Top right figure: Number of hits per layer

Left: number of layer with hits
Electronics commissioning

TOP: first tracks reconstruction, after installation. LHC normal run, ALFA in “garage” mode

Top right: Accumulated hits display on one detector (20 layers), LHC normal run, ALFA in garage mode

Bottom right figure: Reconstructed tracks projection. Double hits reconstruction show up reco outside of the detector area

Plots are Courtesy of ALFA soft team
Detector layer hits during LHC runs, 20 layers in one RP, garage position
Trigger signals Charge measurements (internal LED) for the 8 pots
Installation in LHC Tunnel
• All 8 pots fully operational right after installation in January 2011

• The track signals charge measurement will be installed during 2011 winter shut down (firmware update)

• Connections to the ATLAS CTP and trigger signals timing adjustment performed after installation (commissioning still going on, insertion to the Level 1 ATLAS trigger system)

• Some specific LHC runs with low beta angle are used to commission the detector for physics (in coordination with TOTEM)
ALFA ELECTRONICS

SPARES
Data readout: modified modes

Problem here: the interval is made of 3 successive functions:
1 – MAROC (50ns)
2 – Scan channels (up to 5 = 5us ?)
3 – ADC (500ns)

→ It may exceed the latency time (?)
Trigger QDC readout : modified modes

<table>
<thead>
<tr>
<th>BCID/L1ID</th>
<th>Trigger Charge 1</th>
<th>Trigger Charge 2</th>
<th>Trigger Counters</th>
<th>Trigger Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>12 significant bits</td>
<td>12 significant bits</td>
<td>16 significant bits</td>
<td>16 significant bits</td>
</tr>
</tbody>
</table>

64 bits (4 groups of 16 bits)

T.Count number of bits:

Hypothesis: for an average count per ms the maximum theoretical count is 40K. 16 bits is 65K. There is no minimum count limit.
A realistic number would be 200 (5Khz hit rate, no background)
Electronics commissioning

- No light, HV ON
- Light, ~1 p.e., HV 950V
- Light, ~1 p.e., HV 900V