A 9-Channel, 100 ps LSB Time-to-Digital Converter for the NA62 Gigatracker Readout ASIC (TDCpix)

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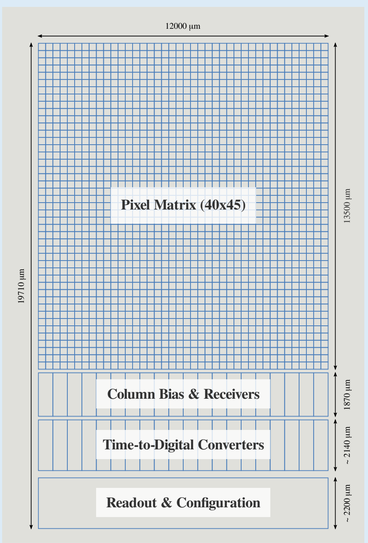
Abstract

The NA62 experiment needs to provide time stamping of individual particles to 200 ps-rms or better per station. Bump-bonded to the pixel sensor each ASIC serves an array of 40 columns x 45 pixels.

Discriminated signals from each pixel are sent to the lower edge of the ASIC to an array of time-to-digital converters (TDCs). The outputs of 5 pixels are multiplexed together yielding a total of 9 channels needed per column. A multilevel approach based on a delay-locked-loop (DLL) is used to achieve a constant time binning of 100 ps over process-voltage-temperature (PVT) variations.

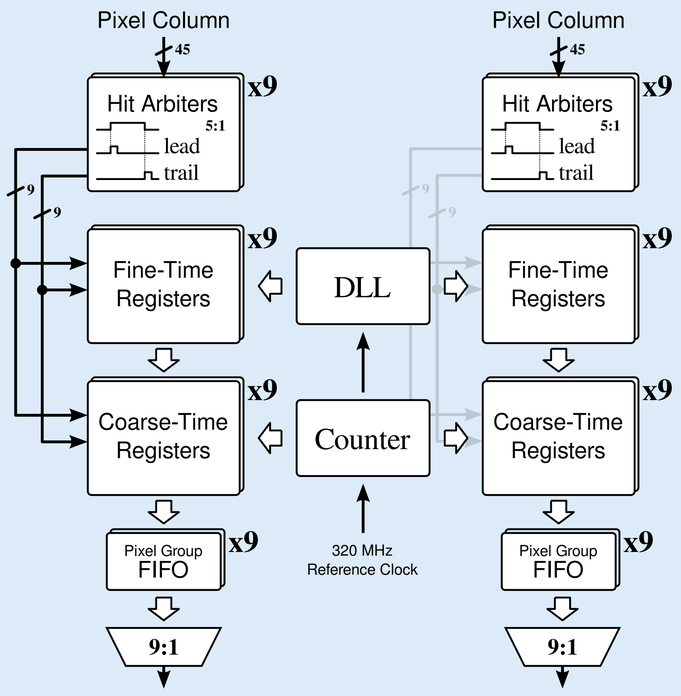
Limited implementation space as well as a large amount of digital logic make the integration especially challenging. Simulation results show that an average rms time resolution of 35 ps and a nominal power consumption of the TDC better than 3.5 mW/channel is achieved. Finally, in the scope of the TDCpix a total of 40 TDCs are embedded to serve all 40 columns.



TDC Architecture

To generate the timing code of the TDC a **multilevel approach** is used. A **DLL** operated at 320 MHz is responsible to generate **fine-time-code** of the TDC. To **increase the dynamic range** of the TDC to 12.8 µs an additional **counter** is used to keep track of the completed clock-cycles.

Each TDC needs to provide **9-Channels** to sample the **leading and trailing edge** of the incoming hit-signals. To **reduce power consumption and area** two adjacent columns share the code-generation circuits.

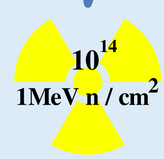


Design Challenges

Small Area: The width of the design is limited by 300 µm.

Noisy Environment: High speed digital logic is implemented on the same substrate.

High Radiation: A yearly dose 10x higher than in CMS inner tracker of LHC.

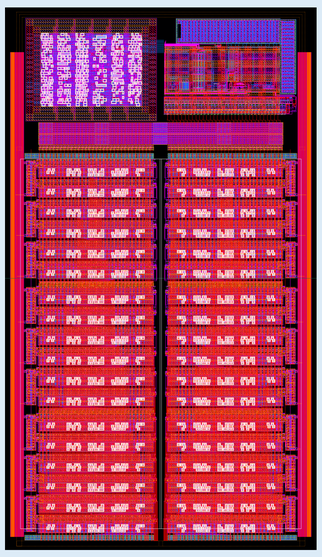


High Resolution: The timing resolution of the TDC needs to be substantially lower than 200 ps.

Low Power: For the full chip an average power of 2 W/cm^2 is not to be exceeded.

Fine Time Resolution Block

Custom Layout

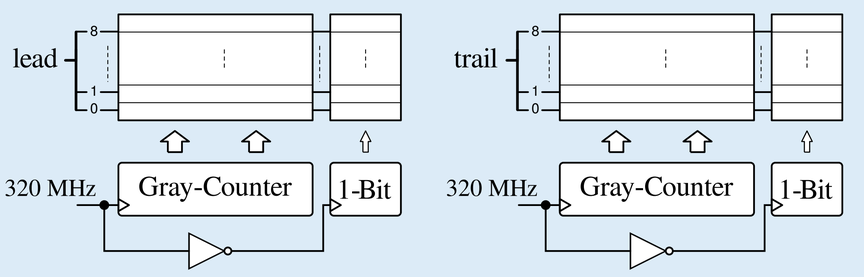


The fine-time-code is generated by a **DLL** running at 320 MHz. Employing a 32 elements in the DLL a minimum bin size of 97.7 ps is achieved. To increase noise-immunity, the **generation** of the fine-time-code is done in a **fully-differential** manner. Anyhow, the **distribution** to the respective hit-registers is accomplished in **single-ended** way to reduce power consumption.

To further **reduce the noise** sensitivity, the DLL and time fine-time registers are sitting on their **own substrate** and are powered on a **separate power supply**.

Coarse Time Resolution Block

Synthesized Logic



Two **gray-code counters** running on the DLL-clock generate the coarse-time stamps for the leading and the trailing edge of the hit-signal respectively.

Upon the asynchronous arrival of the hit-signal the state of the counters are transferred to the respective registers. When latching the state of the counter in its transition region an **ambiguity can occur**. To resolve this ambiguity an **additional bit** - running on the negative edge of the clock - can be used.

Readout & Configuration

In average **each column** produces **126 Mb/s of data** that are to be send out over one **2.4 Gb/s serial interface**. Each interface will serve a total of 10 columns.

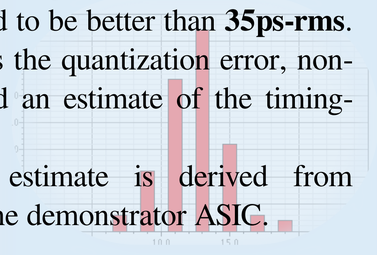
The **configuration** of the TDCpix is accomplished through a custom made **low data-rate serial interface** which is able to configure the respective columns in a hierarchical manner. A (re)-configuration of the TDC can be carried out in a couple of ms.

Performance

Power: Under nominal conditions the TDC consumes **~30 mW/column.** The power is shared equally between the fine- and coarse-resolution block. In total this relates to a power consumption of **3.5 mW/channel**.

Resolution: The **average rms-resolution** of the TDC was simulated to be better than **35ps-rms**. This value includes the quantization error, non-linearity errors and an estimate of the timing-jitter.

The timing-jitter estimate is derived from measurements of the demonstrator ASIC.



Qualification & Testing

To **verify the design** over all process-corners and working conditions extensive analog/mixed-mode simulations have been run. To test the complete scope of the TDC including its analog parts a **full digital verification** will be carried out.

To **ease testing** the un-encoded fine-time code, the phase-detector output and selected codes of the DLL are accessible. The capability of setting the loop bandwidth and to control the bias of the delay-line are further features which increase the testability of the design.