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A 9-Channel, 100ps LSB Time-to-Digital Converter for the NA62 Gigatracker Readout ASIC (TDCpix)

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The NA62 experiment needs to provide time stamping of individual particles to 200ps-rms or better per station. Bump-bonded to the pixel sensor each ASIC serves an array of 40 columns x 45 pixels. Discriminated signals from each pixel are sent to the lower edge of the ASIC to an array of time-to-digital converters (TDCs). The outputs of 5 pixels are multiplexed together yielding a total of 9 channels needed per column. A multilevel approach based on a delay-locked-loop (DLL) is used to achieve a constant time binning of 100ps over process-voltage-
temperature (PVT) variations. Limited implementation space as well as a large amount of digital logic make the integration especially challenging. Simulation results show that an average rms time resolution of 35ps and a nominal power consumption of the TDC better than 3: 5mW /Channel is achieved. Finally, in the scope of the TDCpix a total of 40 TDCs are embedded to serve all 40 Columns. This contribution will present the implementation, simulation results and design challenges of the TDCpix TDC.

Summary 500 words

The NA62 experiment is a new experiment at CERN aiming at measuring the ultra-rare decay of K+ -> pi+ nu nubar. Within the NA62 experiment the Gigatracker is responsible for measurement of the beam. It consists of three independent stations referred to as Gigatracker stations. Each station is composed out of a pixel silicon sensor bump-bonded to a readout ASIC and must provide time stamping of individual particles with a timing resolution better than 200ps-rms. As a proof-of-concept a prototype chip with a single pixel-column was produced and was rigorously tested with highly satisfying results. Based on the experience collected from the prototype a new design is currently under development to implement the full ASIC, named TDCpix. Each ASIC serves a total of 40 columns x 45 pixels.

From the pixel matrix the discriminated hit signals are transmitted to the end of column region to an array of 40 time-to-digital converters (TDCs). In each case 5 pixels are grouped to feed one channel of a TDC to measure the leading and the trailing edge time of the hit signal. There is one 9-channel TDC per column where two neighboring TDCs are sharing resources.

The TDC itself uses a 320 MHz clock in conjunction with a 32-element delay-locked-loop (DLL) to achieve a constant timing accuracy over process-voltage-temperature (PVT) variations of 100ps-LSB. To extend its dynamic range to several microseconds the TDC uses a counter to keep track of the clock cycles. A synchronization concept based on a single counter using 1 single additional bit is proposed. On the arrival of a hit signal, the state of the DLL and the counter is stored. Due to the high data rate, the state of the DLL is encoded to 5-bit to be read out in parallel. A state machine as well as a set of configuration registers is responsible for controlling the state of the TDC. Due to the high radiation exposure, a triple redundant configuration scheme and triplicated logic is employed to reduce errors due to single event effects.

In total a set of forty 9-channel TDCs are to be implemented per chip. This in turn requires a careful qualification of the TDC performance over different corners and different sets of parameters. Simulation results show that the TDC 3-sigma rms-timing-resolution, which includes quantization-error, non-linearities and jitter (measured from the prototype), ranges from 31ps to 39ps and that the power consumption per channel is better than 3.5mW. Particularly challenging for the design is the restriction in physical space as well as the noisy environment due to a large amount of digital logic.

This contribution will present important aspects of the implementation of the TDCpix TDC focused on the critical aspects related to the constraints given by the experiment. Simulation results as well as the methodology followed to qualify the design will be presented.

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