Update on the high speed serializer ASIC development for ATLAS Liquid Argon calorimeter upgrade

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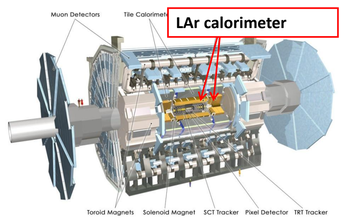
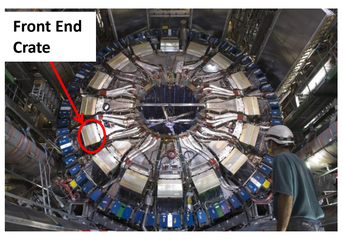
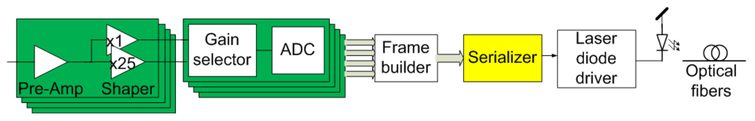
Introduction

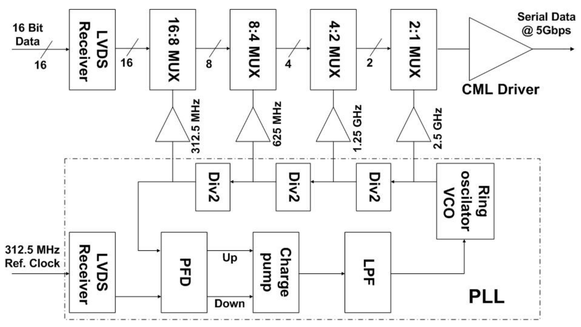
- The data rate of the optical links proposed for the ATLAS LAr calorimeter upgrade increases from 1.6 Gbps to about 100 Gbps per front-end board (FEB) [1].
- The front-end electronics, including the optical links on the transmitter side, is exposed in a harsh radiation environment.
- The data rate of the serializers currently used in high energy physics experiments is too slow for the ATLAS LAr upgrade
- For the ATLAS LAr upgrade, a high speed radiation tolerant serializer ASIC is required.
- We have been developing a serializer application-specific integrated circuit (ASIC) based on a commercial 0.25-μm silicon-on-sapphire (SoS) CMOS technology. The first prototype , a 5 Gbps 16:1 serializer (dubbed as LOCs1) has been designed, fabricated, and tested [2]. The second prototype, a double-lane, 8 Gbps per lane serializer (dubbed as LOCs2) is under development.



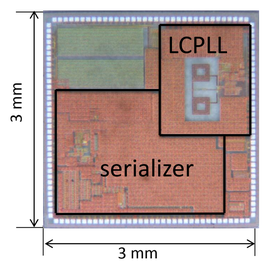




The design of single-lane serializer ASIC



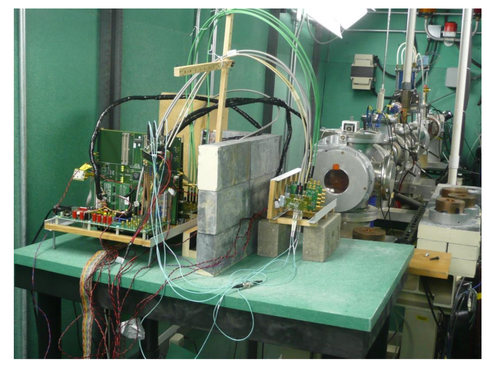
Block diagram of the serializer LOCs1



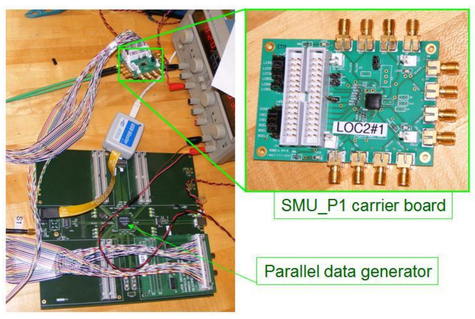
Die micrograph

Average values of the measured parameters

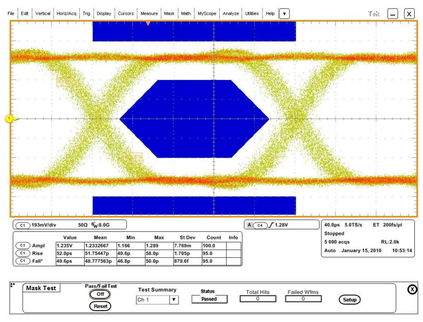
Output amplitude (peak-peak, V)	1.16
Rise time (20% - 80%, ps)	52.0
Fall time (20% - 80%, ps)	51.9
Total jitter @ BER 10^{-12} (peak-peak, ps)	61.6
Random jitter (RMS, ps)	2.6
Deterministic jitter (peak-peak, ps)	33.4
Power consumption (mW)	463
Minimum data rate (Gb/s)	4.0
Maximum data rate (Gb/s)	5.7



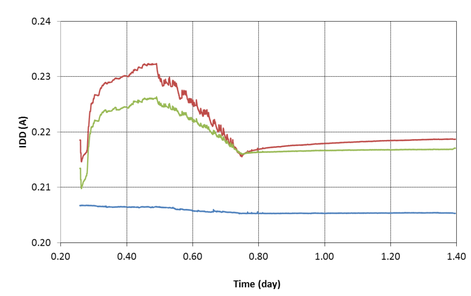
Setup of radiation test



Pictures of the test setup

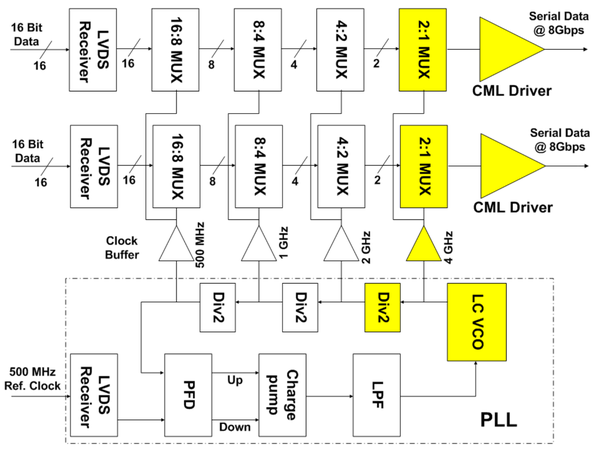


Eye diagram at 5 Gbps



The power supply current change during the test and during annealing time

The design of double-lane serializer ASIC

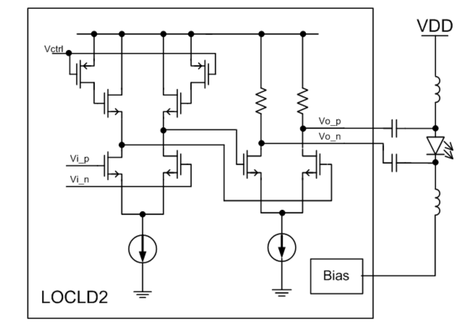


Block diagram of LOCs2

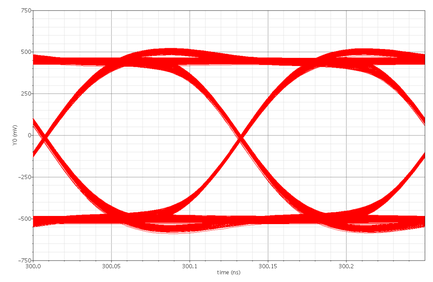
Design status of LOCs2

Parts	Layout	Area (μm²)	Power (mW)	Performance
VCO		500x900	4.5	Implemented and tested [3]. Tuning range is 3.7 ~ 5.0 GHz
Divider (÷2)		50x50	5.3	Max operation freq. > 4.25 GHz in the worst corner and 85 °C
Clock buffer		40x50	8.0	Max operation freq. > 4.9 GHz in the worst corner and 85 °C
2:1 Multiplexer		90x90	13.3	Deterministic jitter < 5.6 ps) w/ 8 Gb/s PRBS7 signals in the worst corner and 85 °C
CML driver		700x700	70	Deterministic jitter < 12 ps with 8 Gb/s PRBS7 signals in the worst corner and 85 °C

The double-lane 8-Gbps serializer will be submitted in the beginning of 2012.



The last two stages of the laser driver (LOCLD2)



Eye diagram of LOCs2+LOCLD2 at 8 Gbps in post layout simulation

Conclusion

To meet the challenge of the ATLAS LAr calorimeter upgrade, we have been developing a serializer ASIC based on a commercial 0.25-μm SOS CMOS technology. The first prototype, a 5 Gbps 16:1 serializer has been designed, fabricated, and tested in lab environment and in 200 MeV proton beam. The test results indicate that the first prototype meets the design goals. The second prototype, a double-lane, 8 Gbps per lane serializer is under development. The post layout simulation indicates that 8 Gbps is achievable.

Acknowledgments

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References

1. Hucheng Chen, Readout Electronics for the ATLAS LAr Calorimeter at HL-LHC, the Technology and Instrumentation in Particle Physics (TIPP) conference, Chicago, U.S.A, June 9-14, 2011.
2. Datao Gong, A 16:1 Serializer ASIC for Data Transmission at 5 Gbps, 2010 JINST 5 C12009.
3. Tiankuan Liu *et al*, The Design of a High Speed Low Power Phase Locked Loop, 2010 *JINST* **5** C12045.

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