A Reticle Size CMOS Pixel Sensor Dedicated to the STAR HFT

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ABSTRACT: ULTIMATE is a reticle size CMOS Pixel Sensor (CPS) designed to meet the requirements of the STAR pixel detector (PXL). It includes a pixel array of 928 rows and 960 columns with a 20.7 µm pixel pitch, providing a sensitive area of ~3.8 cm². Based on the sensor designed for the EUDET beam telescope, the device is a binary output sensor with integrated zero suppression circuitry featuring a 320 Mbps data throughput capability. It was fabricated in a 0.35µm OPTO process early in 2011. The design and preliminary test results, including charged particle detection performances measured at the CERN-SPS, are presented.

KEYWORDS: reticle size CMOS Pixel Sensors (CPS); Correlated Double Sampling (CDS); zero suppression; fast readout.

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1. Introduction

The tracking performances of CMOS Pixel Sensors (CPS) are now well established and the sensors are foreseen to equip several vertex detectors. The STAR HFT (Heavy Flavor Tracker) has generated the first vertex detector based on CPS. The pixel detector (PXL), composed of two layers of high resolution CPS, is presently being fabricated.

This development began more than eight years ago in collaboration with LBNL. Three generations of sensors have been designed at IPHC. The first generation sensor featured analogue outputs (MimoSTAR-1, -2 and -3) and did not integrate signal processing circuitry. A 3 sensors beam telescope has been constructed with MimoSTAR-2 and operated inside the STAR apparatus near the RHIC beam in 2007 [1]. It was the first test of the CPS technology in a collider environment. The second generation sensors (PHASE-1 and PHASE-2) have reticle dimensions and binary outputs, but no integrated zero suppression logic. In 2012, an engineering prototype detector with limited coverage (1/3) will be installed in the experiment, equipped either with PHASE-1/-2 sensors or with those of the third generation. The latter is represented by the ULTIMATE sensor, which was designed to fulfil all STAR-PXL specifications (cf Table 1), in particular those concerning the hit rate (200-300 hits/sensor for an integration time $\leq$ 200 μs), the spatial resolution (~ 6-8 μm), the power consumption ($\leq$150 mW/cm²), the radiation tolerance (~ 150 kRad and few 10^{12} MeV n_{eq}/cm^2 per year) and the operation at room temperature (~ 30-35 °C). The final detector, composed of two complete layers populated with 400 ULTIMATE sensors in total, will be installed in 2013.

This contribution will discuss the design of the ULTIMATE sensor with its optimisation approaches, and show its test results, including charged particle detection performances measured at the CERN-SPS.

STAR-PXL Detector	Sensors requirements
Sufficient resolution to resolve the secondary decay vertices from the primary vertex	Sensor spatial resolution < 10 µm
Multiple scattering minimisation X/X_0 = 0.37 % per layer	Sensors thinned to 50 µm, mounted on a flex kapton, aluminium cable
Luminosity = 8x10^{27} /cm^2 /s at RHIC	~ 200-300 hits/sensor (~ 4 cm^2) in the integration time window (≤ 200 µs)
Low mass in the sensitive area of the detector => airflow based system cooling	Sensor work at ambient temperature (~ 30 - 35°C) Power dissipation ≤ 150 mW /cm^2
Sensors positioned close to the interaction region (2.5 – 8 cm radii)	Radiation environment: ~ 150 kRad /year, few 10^{12} n_{eq} /cm^2 /year

Table 1: Sensor requirements in STAR-PXL detector.

2. ULTIMATE sensor design and optimization

ULTIMATE is a full reticle size (~2x2 cm^2) sensor with binary output and integrated zero suppression logic. Its main characteristics are similar to those of the MIMOSA-26 sensor, fabricated in 2009 for the EUDET beam telescope [2]. The design has incorporated the test results of MIMOSA-26 and has been optimised for the STAR environment.

The block diagram of ULTIMATE is presented in Figure 1 (left). It includes a pixel array of 928 rows and 960 columns with 20.7 µm pixel pitch, covering a sensitive area of ~ 3.8 cm^2. The integration time is 185.6 µs.

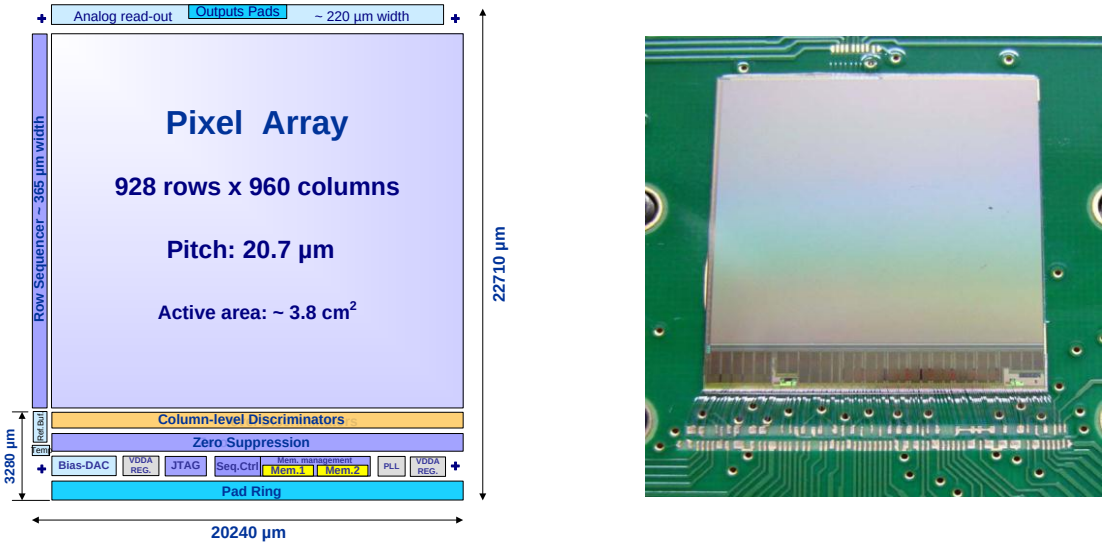

Figure 1: Functional block diagram of ULTIMATE (left) and Picture of the sensor on its PCB (right).

The architecture is based on a column parallel readout with amplification and correlated double sampling (CDS) inside each pixel. Each column is ended with a high precision discriminator [3] and is read out in a rolling shutter mode at 5 MHz (200 ns/row). The 960 discriminators are sub-divided into 4 groups of 240 discriminators (corresponding to sub-matrices called A, B, C, D hereafter). Their outputs are processed through an integrated zero suppression micro-circuit, which results are stored in two SRAM according to a ping-pong arrangement allowing for a continuous readout. This architecture is capable to cope with a hit rate of 10^6 hits/cm^2/s. The sparsed data are multiplexed onto two LVDS outputs at 160 MHz.

The on-chip programmable bias DACs, the threshold voltages for the groups of discriminators, the test mode selection are set via a JTAG controller. An on-chip voltage regulator is used to provide the pixel clamping voltage (Vcl in Fig.2) in order to minimise interferences on this critical node. Individual blocks, like PLL and voltage regulators for analogue power supply, were designed for test purposes [4, 5].

2.1 Pixel optimization

The active area of ULTIMATE is nearly twice the one of MIMOSA-26. As the sensor is operated at a room temperature of 30–35 °C in the STAR experiment (air cooling), the chip power dissipation is limited to ~150 mW/cm^2. In order to achieve this goal, the pixel pitch was enlarged from 18.4 µm to 20.7 µm, therefore decreasing the number of columns (960) with respect to MIMOSA-26 (1152). The change in pitch size expresses a trade-off between power consumption, non-ionising radiation tolerance and spatial resolution. It was validated by a small prototype, called MIMOSA-22AHR, submitted in April 2010, featuring the two pitch values, different amplifiers designs and sensing diodes, which were assessed by extensive tests. Taking into account the characterisation results of this chip, the schematic of the pixel retained for ULTIMATE is represented in Figure 2 [6]. An adaptative feedback was used to stabilise the operating point of the common source amplifier. In this way, working conditions can be guaranteed for all pixels (~10^6) w.r.t. temperature changes, irradiation and process parameters variation. The load transistor of the amplifier (M2) biased with transistor (M3) allows increasing the AC gain by about a factor of two, improving thus the signal-to-noise ratio. The pixel layout has been carefully optimised for parasitics and the feedback transistor (M4) was replaced by its enclosed layout variant (w.r.t. MIMOSA-26) for the sake of radiation tolerance.

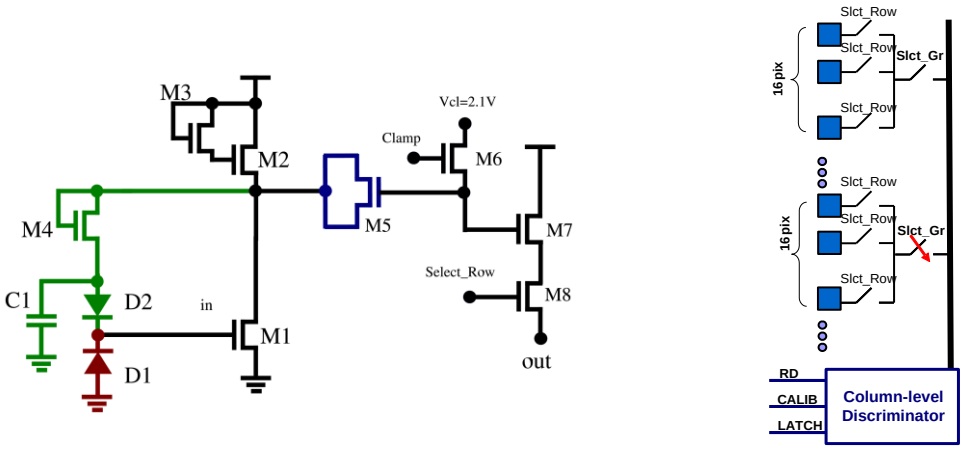

Figure 2: Schematics of a pixel and a column of pixels connected to the discriminator.

Furthermore, in order to ensure that the pixel signal is stabilised in the two sampling phases (CDS) of the readout sequence, each column is split into 58 groups of 16 pixels (cf Fig.2), thus reducing the capacitance of the output node (~ 4 pF). The transistors sizes of the pixel output stage (M7, M8 and M_{slct_gr}) were optimised to minimise the time constant in the worst case for a current value of 50 µA.

In the STAR-PXL design, where the detector may be replaced within 8 hours, the sensor has to stay operational after an exposure of 150 kRad and a few 10^{12} n_{eq}/cm^2 irradiation doses. In order to guarantee its non-ionising radiation tolerance, the sensor was fabricated with a

substrate featuring a high-resistivity epitaxial layer (≥ 400 Ω.cm). The benefit of the latter was evaluated with the MIMOSA-26 sensors fabricated with low and high resistivity epitaxial layers. Test results are summarised in Table 2.

EPI layer	Standard (~10 Ω·cm) 14 µm		High resistivity (≥ 400 Ω·cm)		
	Before irradiation	After 6x10 ^{12} n_{eq}/cm²	EPI thick	Before irradiation	After 6x10 ^{12} n_{eq}/cm²
S/N at seed pixel (^{106}Ru source)	~ 20 (230 e$^-$/11.6 e$^-$)	10.7	10 µm	~ 35	22
			15 µm	~ 41	28
			20 µm	~ 36	----------

Table 2: Signal-to-noise ratio (most probable value) for the seed pixel of clusters generated by beta particles emitted by a ^{106}Ru source. The measurements were performed at room temperature and are shown before irradiation and after exposure to a fluence of 6x10^{12} n_{eq}/cm². The left side of the table corresponds to a 14 µm thick, low resistivity, epitaxial layer, while the right part stands for high resistivity epitaxial layers of 10, 15 and 20 µm thickness.

2.2 Digital conception challenges

The size of the sensor (~2x2 cm^2) and the layout constraint represent a conception challenge for the digital control circuit of ULTIMATE in terms of combined speed and power consumption. The features of the digital part are similar to those of MIMOSA-26 [7]. After A/D conversion, the digital signals are processed in parallel in 15 banks of 64 columns by the zero suppression circuit, and next arranged and stored in a memory row by row.

The main changes and blocks optimisation w.r.t. MIMOSA-26 are summarised hereafter:

- The memories depth was increased from 600 to 2048 words to cope with the higher hit density.
- The length of the pixel row sequencer control was extended by a factor of nearly two, imposing to the row control signals to be uniformly distributed with less than 500 ps dispersion.
- The output data frequency was increased from 80 to 160 MHz, imposing a check of all critical paths of the data serializer for all operation conditions.

2.3 On-chip regulator design

A voltage regulator was designed to generate the pixel clamping voltage (V_{cl}) in the chip [8]. The goal is to reduce the number of tracks on the ladder flex cable for the sake of material budget and to eliminate the crosstalk between the sensors of a ladder. The schematic and the layout of the regulator are presented in Figure 3. Its characteristics are summarised in Table 3.

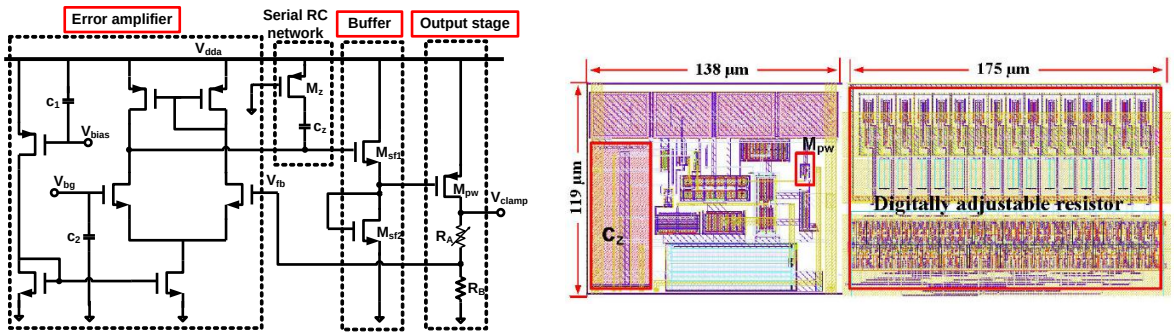

Figure 3: Schematic of the regulator (left) and its layout (right).

Capacitive load	> 5 nF
Consumption	< 1 mW
Output voltage range	1.9-2.3 V
Noise	74.8 nV/√Hz at 1 kHz
PSRR	52 dB at 10 kHz 38 dB at 1MHz

Table 3: Characteristics and simulated results of the regulator.

The regulator was first implemented and tested in the small prototype MIMOSA22-AHR. Its noise contribution remains small (< 10 %) and was reduced (to 3 %) in ULTIMATE by using a filter capacitance of a few nF (estimated parasitic capacitance on the pixel clamping line).

3. Test results

ULTIMATE was submitted to fabrication by the end of January 2011 in a CMOS 0.35 µm OPTO process. Two wafers, one with a 15 µm thick epitaxial layer and the other with a 20 µm thick epitaxial layer, diced and thinned down to 120 µm, were received at the laboratory early April 2011. The wafer with 15 µm thick layer was then thinned down to 50 µm.

3.1 Laboratory test results

The sensors were first tested in the laboratory in analogue output mode at low frequency, 40 MHz (digitization and CDS done via off-line data analysis). The chips were illuminated with a ^{55}Fe source in order to assess the pixel noise, the charge collection efficiency (CCE) and the uniformity of the pixels response. The source was also used to calibrate the charge-to-voltage conversion factor. Figure 4 displays the noise level of all pixels composing one of the sensors with 20 µm thick epitaxial layer. One observes a good noise uniformity across the ~ 4 cm^2 active area. The average noise value amounts to ≤ 15 e$^-$ ENC at 20°C and 40 MHz readout clock frequency. The pixel gain is around 65 µV/e$^-$.

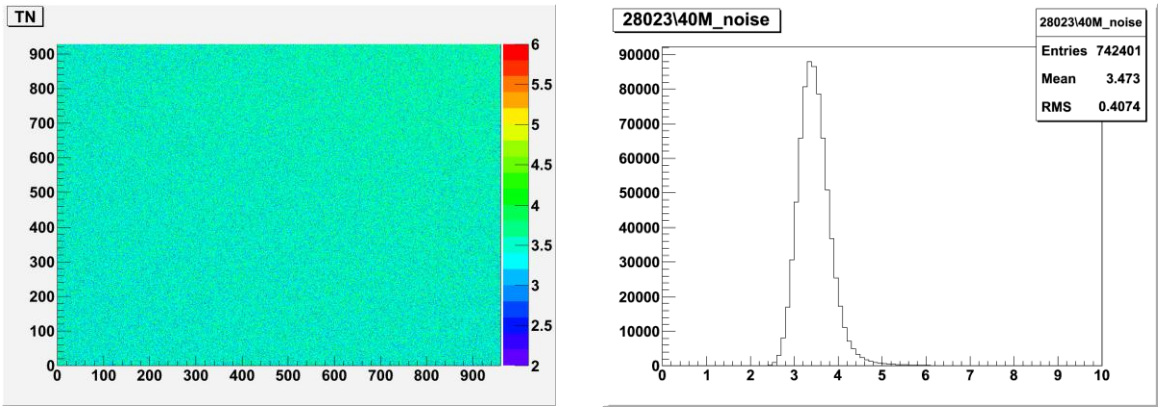

Figure 4: Distribution of the pixels noise over the full sensitive area of ULTIMATE at 40 MHz clock frequency (left) and Histogram of pixels noise in ADC units (right) (1 ADC unit =4.15 e$^-$).

The CCE was derived from the clusters generated by the X-Rays emitted by the source. The seed pixel of each cluster was defined as the one having collected the largest charge. Next, groups of 2x2, 3x3 and 5x5 pixels were built, where the 2x2 group was the one having collected

the largest charge among the four possible groups one can built around the seed pixel. The most probable value for the distribution of the charge collected in the clusters divided by the calibration peak value determines the cluster CCE. The measured values are shown in Tables 4 and 5 as a function of the temperature and for two values of analogue power supply (Vdda), respectively. One observes that the CCE is weakly sensitive to temperature and nearly insensitive to the considered analogue power supply variations. The analogue power supply dependence was studied for power saving purposes.

Ultimate Sensor Temperature	***Calib peak (U_{ADC})***	***ENC (e-)***	***CCE***			
			Seed pixel	***2x2 pixels***	***3x3 pixels***	***5x5 pixels***
~20 °C	*395*	*13.8*	*24%*	*62%*	*82%*	*94%*
~35 °C	*385*	*16.4*	*24%*	*62%*	*83%*	*96%*
~45 °C	*369*	*20.7*	*23%*	*63%*	*85%*	*99%*

Table 4: Calibration peak charge, noise and CCE measurements as a function of the temperature at Vdda=3.3 V.

Analog Power Supply	***Calib peak (U_{ADC})***	***ENC (e-)***	***CCE***			
			Seed pixel	***2x2 pixels***	***3x3 pixels***	***5x5 pixels***
Vdda = 3.3V	*395*	*13.8*	*24%*	*63%*	*82%*	*95%*
Vdda = 3V	*390*	*13.9*	*24%*	*62%*	*83%*	*95%*

Table 5: Calibration peak charge, noise and CCE measurements at ~20°C for two values of analogue power supply.

In the next step, the digital outputs were tested in the configuration where all discriminators are connected to the pixel array. Figure 5 (left) displays the response of a group of 240 discriminators as a function of the threshold value. The slope of the transition and its dispersion were interpreted in terms of fixed pattern noise (FPN) and temporal noise (TN). Their values are shown in Figure 5 (right) and the noise measurements for each group of discriminators are summarised in Table 6.

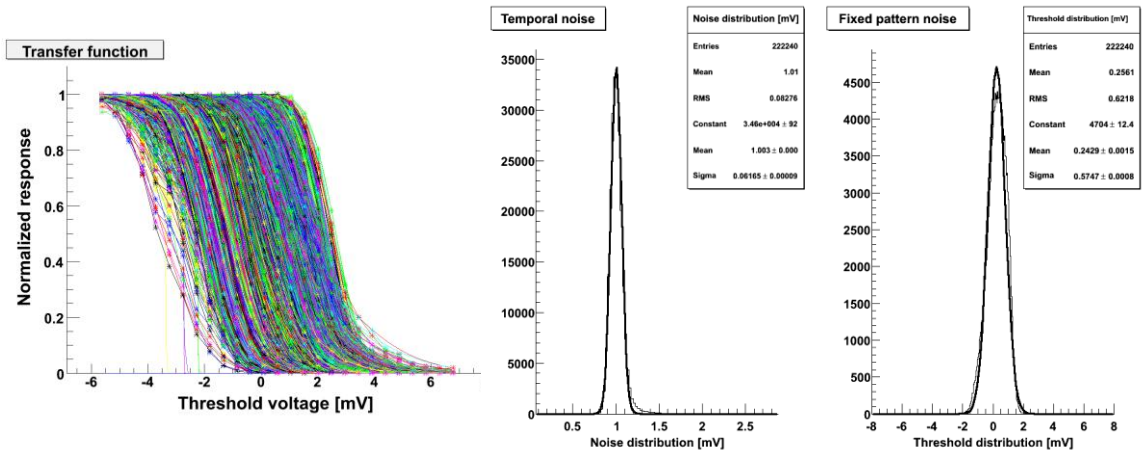

Figure 5: Transfer function (left), TN and FPN (right) of a group of 240 discriminators (sub-matrix A) measured at 15°C.

	Sub-matrix A (Col 1-240)	**Sub-matrix B** (Col 241- 480)	**Sub-matrix C** Col 481 – 720)	**Sub-matrix D** Col 721 -960
Temporal Noise (mV)	1	0.95	0.92	0.9
Fixed Pattern Noise (mV)	0.57	0.49	0.48	0.47

Table 6: Measured Temporal Noise and Fixed Pattern Noise for each group of 240 columns called sub-matrix A, B, C and D.

The TN amounts to ~ 0.9–1 mV and the FPN amounts to ~ 0.47-0.57 mV. These values are slightly higher than those observed with MIMOSA-26, but they comply with the PXL requirements. The reason for this noise increase is currently being investigated.

The power consumption of the sensor was measured and found to be ~ 730 mW for the whole chip for a power supply of 3.3V, which corresponds to 158 mW/cm^2, in agreement with the simulation.

Finally, over 19 tested sensors, 14 are fully functional and 5 present ~ 1 % of dead pixels, indicating that the fabrication yield is satisfactory.

3.2 Beam test results

The performances of the ULTIMATE sensors were evaluated with a ~120 GeV π^- beam at the CERN-SPS. Six sensors with 20 µm high-resistivity epitaxial layer were exposed to a dose of 150 kRads. The measurements were performed at 15 and 30 °C before and after irradiation with an analogue power supply of 3.3 V. The measurements were repeated at 3.0 V.

The observed performances are shown in Figures 6 and 7 as a function of the discriminators' threshold. The figures display the particle detection efficiency, the single point resolution and the fake hit rate. The latter expresses the probability for pixels to generate a noise fluctuation above threshold. In Figure 7, the performances are displayed before and after irradiation, measured at 30 °C and for Vdda= 3V.

An efficiency above 99.5 % was obtained for a very low average fake hit rate (< 10^{-4}). The single point resolution is better than 4 µm. The performances of ULTIMATE remain almost unchanged when lowering the analogue power supply to 3 V. Operating the sensor with Vdda at 3 V allows mitigating by 6 % the total power consumption, thus reducing it below 150 mW/cm^2.

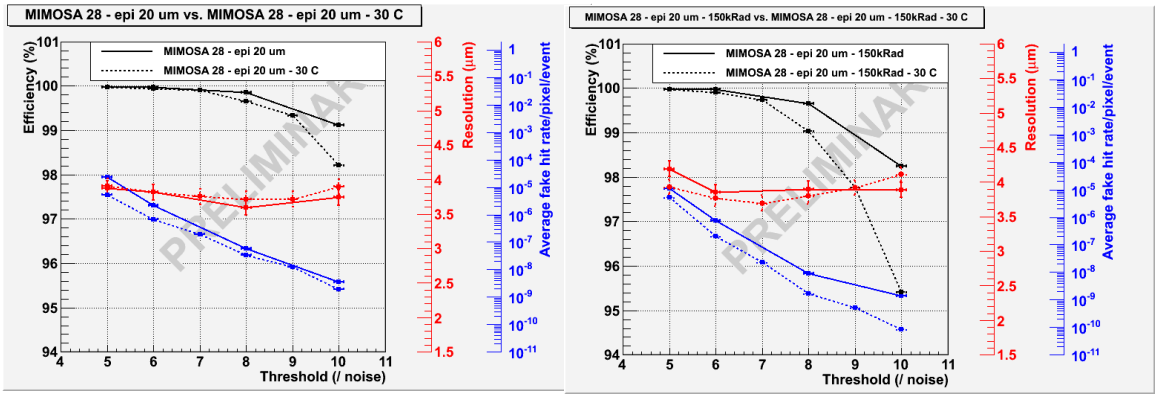

Figure 6: Performances of the ULTIMATE sensor with 20 µm thick epitaxial layer, measured at 15 and 30 °C and for Vdda= 3.3 V, before (left) and after (right) exposure to a dose of 150 kRads.

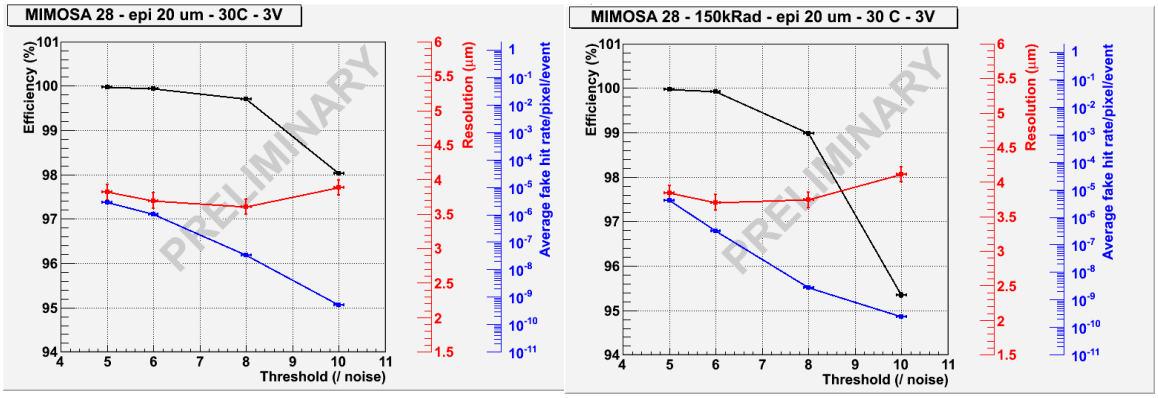

Figure 7: Performances of the ULTIMATE sensor with 20 µm thick epitaxial layer, before (left) and after (right) exposure to a dose of 150 kRads, measured at 30°C and for Vdda= 3V.

The influence of the epitaxial layer thickness on the sensor detection performances is under study, based on test beam data of sensors fabricated with either a 15 or a 20 µm thick layer. Present results show that both sensors exhibit very similar values of the detection efficiency, fake rate and spatial resolution for nearly all operating conditions investigated up to now.

4. Conclusion and perspectives

A reticle size CMOS sensor with integrated sparsification has been fabricated for the upcoming vertex detector (PXL) of the STAR experiment at RHIC. The detection performances of 50 µm thin sensors have been assessed with minimum ionising particles, in operating temperature and ionising radiation conditions reflecting those of the STAR-PXL inner layer.

A detection performance of nearly 100 % was found for a wide range of threshold values of the 960 discriminators integrated in the chip, for which a very modest fake hit rate was observed ($<10^{-4}$). These very satisfactory results were complemented with a single point resolution in the 3.5-4.0 µm range. Finally, due to the rolling shutter read-out architecture of the sensor, the power consumption was kept around 150 mW/cm^2, translating into about 0.8 µW per pixel. All these results comply with the STAR-PXL specifications. The yet missing performance test concerns the non-ionising radiation tolerance, which should amount to 3 10^{12} n_{eq}/cm^2, and which is under way and was actually already verified with a small prototype.

Based on these results, a pre-production has been realised, which provides the set of sensors needed for the engineering prototype detector, which is scheduled for installation on beam at the end of 2012. This first step is supposed to be followed by the assembly and commissioning of the final detector in through 2013, in perspective of the physics program studying AuAu collisions foreseen in 2014.

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