A fast and low noise charge sensitive preamplifier in 90 nm CMOS technology

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Overview

An integrated charge sensitive preamplifier (CSP) was realized in a TSMC 90 nm CMOS technology. The work is part of the R&D effort towards the read out of pixel sensors in next generation HEP experiments. The CSP was designed to read out pixels of 1 pF capacitance with a signal rise time below 2 ns (requiring a closed loop bandwidth of about 200 MHz) and a noise below 500 electrons RMS. Also larger pixels of up to 5 pF capacitance need to be read out, with a rise time still below 5 ns.

Layout

The CSP die size is 300 μm x 250 μm (including two power supply bypass capacitors of a few pF). The layout was not optimized for compactness.

Signals

The response of the prototype to a charge pulse of 15k electrons is shown. The source simulates a pixel with 1 pF capacitance (C\textsubscript{d}). The signal is acquired at the far end of an AC coupled 50 Ω transmission line.

Noise

The equivalent noise charge (ENC) was measured as the RMS baseline fluctuation at the CSP output, divided by the charge gain. The main source of parallel noise is the feedback resistor, contributing with about 200 electrons RMS, regardless of the pixel capacitance. The main source of series noise is the the input transistor, with 1 nV / √Hz at high frequency, giving about 100 electrons RMS for pixels of 1 pF capacitance, directly proportional to the pixel capacitance. To a first order approximation, the 1/f noise components do not contribute, because the signal is AC coupled at the output with a high pass at about 1 MHz. By applying an offline RC filter with varying filter time constants up to 100 ns the series noise contribution could be reduced.

Conclusions

The chip performs well in terms of bandwidth and noise, meeting the design specifications. The adopted 90 nm CMOS technology allows to achieve very high transconductance thanks to increased scaling. Low series noise can be obtained, although at the price of fairly high power consumption in the 1st stage. Some power could be saved in the output stage if the 50 Ω line drive capability is not required. The value of the feedback resistor could be increased to reduce the parallel noise. The silicon realization was possible thanks to the INFN To_Asic program.