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A fast and low noise charge sensitive preamplifier in 90 nm CMOS technology

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An integrated charge sensitive preamplifier was designed in 90 nm CMOS technology. The chip is part of the R&D effort towards the upgrade of the pixel sensors of the CMS detector. It was submitted in april 2010, and was received and tested in autumn 2010.
In the design of the amplifier block, a single ended structure was preferred over a differential one, in order to achieve a lower noise. Three gain stages were put in series to obtain a high open loop gain at high frequency. The gain of the third stage was made adjustable, in order to change the overall open loop gain to match the closed loop gain.
Thanks to the high speed MOS transistors and low parasitic capacitances, the feed-backed preamplifier can operate at a frequency above 100 MHz, with transistion edges of about 5 ns. The input-referred RMS noise is 400 eˆ- with a 1 pF detector over the full preamplifier bandwidth, allowing to read out charge pulses of a few keˆ-.
Power consumption is less than 5 mW for the single channel prototype.

Summary 500 words

An integrated charge sensitive preamplifier was designed in 90 nm CMOS technology from TSMC. The chip is part of the R&D effort towards the upgrade of the pixel sensors of the CMS detector at the LHC. It was realized in the framework of the TOASIC project of the Italian Institute for Nuclear Physics (INFN). The chip was submitted in april 2010, and was received and tested in autumn 2010.
The approach is that of the classic charge sensitive preamplifier: a high gain amplifier having the parallel combination of a capacitor and a resistor in the feedback loop. The feedback capacitor was set to 50 fF, while the feedback resistor was set to 250 kOhm. The value of the feedback resistor is low because the preamplifier was designed for fast operation; thus a low feedback resistor allows to discharge the preamplifier quickly, and its noise contribution is not expected to dominate because of the short pulse duration.
In the design of the amplifier block, a single ended structure was preferred over a differential one, in order to achieve a lower noise. The low supply voltage (1.2 V) compared to the MOS thresholds (about 300 mV for large area transistor) disfavours the use of structures such as cascodes. To obtain a high open loop gain in this technology, which features MOS transistors with high transconductance but low output impedance, three gain stages were put in series. The gain of the third stage was made adjustable, in order to change the overall open loop gain to match the closed loop gain, which is determined by the detector capacitance.
Thanks to the high speed MOS transistors and low parasitic capacitances, the feed-backed preamplifier can operate at a frequency above 100 MHz, with a transistion edge of 5 ns for smaller signals (about 10 keˆ-, or 1.6 fC), reducing to less than 4 ns for larger signals (> 100 keˆ-, or 16 fC).
The input-referred noise spectral density is less than 1 nV/sqrt(Hz) at high frequency, and the RMS noise is 400 eˆ- with a 1 pF detector, over the full preamplifier bandwidth. If a shaping filter is applied after the preamplifier, the noise performance can be improved, allowing to read out charge pulses of a few keˆ-.
Thanks to the fast response and the low noise, a jitter below 50 ps was measured for large signals (150 keˆ-, or 24 fC).
The output stage in class A was designed to drive a 50 ohm transmission line.
The design was optimized for pixels of 1 pF capacitance; however, thanks to a design feature, also detectors of larger capacitance, up to about 5 pF, can be read out without a significant loss in bandwidth (although noise becomes larger).
The gain vs input charge curve shows a smooth saturation; this, combined with the low noise, allows a wide dynamic range to be handled by the preamplifier. The preamplifier was tested with charge pulses ranging from 5 keˆ- (0.8 fC) up to 300 keˆ- (50 fC).
Power consumption is less than 5 mW for the single channel prototype.

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