The NA62 LAV front-end electronics

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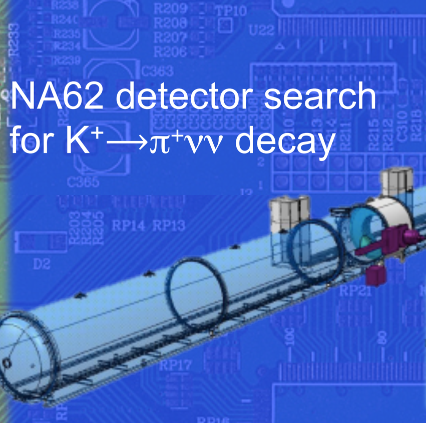
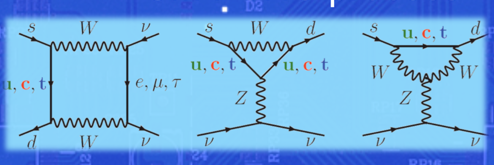
NA62 detector search for $K^+ \to \pi^+ \nu\nu$ decay

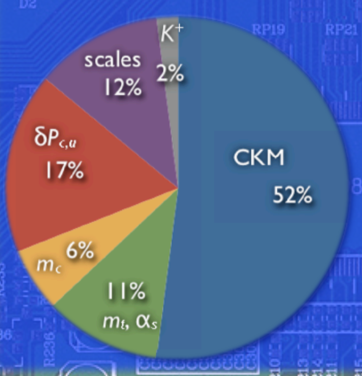


SM FCNC process



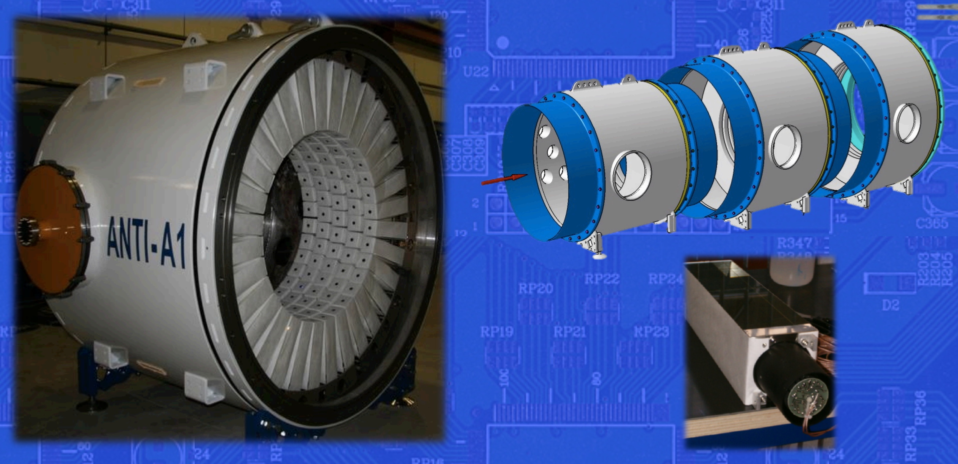
Decay	Short dist.	Theo. BR	Exp. BR
$K^+ \to \pi^+ \nu\nu$	88%	$(8.22\pm0.75)\times10^{-11}$	$(1.7\pm1.1)\times10^{-10}$
$K^0_L \to \pi^0 \nu\nu$	99%	$(2.76\pm0.40)\times10^{-11}$	$<2.6\times10^{-8}$ 90%

- ☑ Ultra-rare FCNC process, forbidden in SM at tree level
- ☑ Dominant (88%) short-distance contribution
- ☑ Theoretical SM BR calculable with ~9% precision
- ☑ Very sensitive to physics beyond the SM



9% theoretical uncertainties dominated by errors on CKM elements and top mass. Thanks to LHC and new B factories error will probably decrease to ~6%

NA62 Large Angle photon Veto detectors



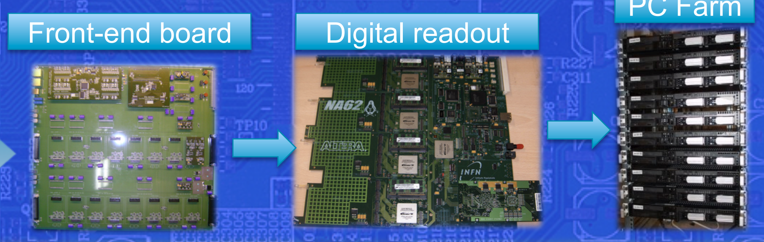
- ☑ Designed to reject π^0 from $K^\pm \to \pi^\pm \pi^0$ decays with 10^{-8} inefficiency
- ☑ 12 stations along a 80-meter decay region
- ☑ 2496 lead glass blocks from OPAL EM calorimeter
- ☑ 4-5 rings per station (>20 X_0) maximize geometrical shower containment
- ☑ Single station inefficiency for γ detection ~10^{-4} down to 100-200 MeV
- ☑ Operation in vacuum: O(10^{-6}) mbar

NA62 Large Angle Veto readout chain

LAV station

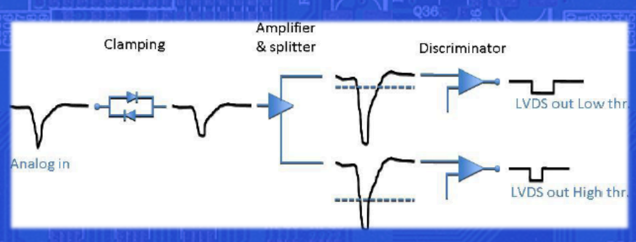
- ☑ 2496 readout channels in 12 stations
- ☑ ~ 100 KHz max rate per channel
- ☑ Time resolution <1ns, energy resolution <10% at 1 GeV

Front-end board → Digital readout → PC Farm

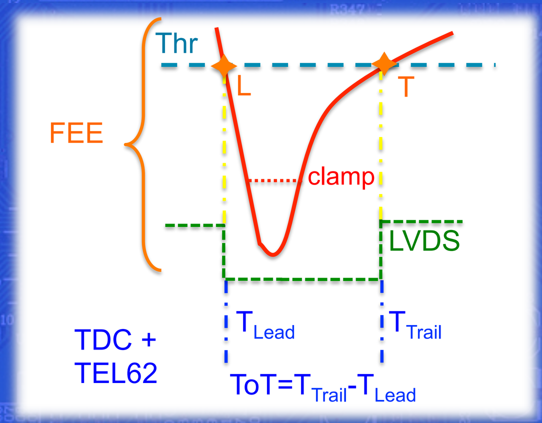


FEE working principle

From analog signal to ToT

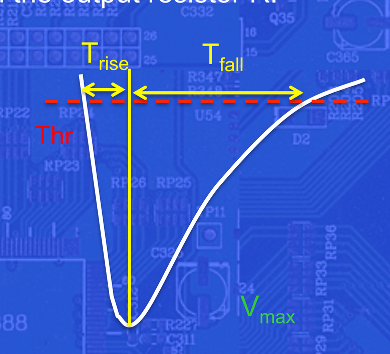


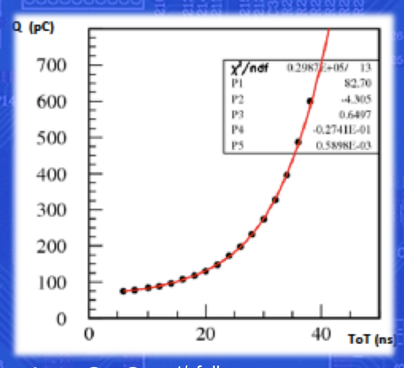
- ☑ Split the input signal in two copies
  - 1 copy to comparator + 1 copy to analog sums
- ☑ Clamp the signal preserving its width
- ☑ Amplify the signal x3 to restore the overdrive
- ☑ Compare the signal with 2 different thresholds
  - Each thr is independently adjustable 0-250mV
- ☑ Produce an LVDS signal and send the signal to the digital read out board
- ☑ Measure the leading and trailing times of the LVDS signal and compute the ToT = $T_{Trail}-T_{Lead}$



Charge reconstruction algorithm

The ToT is the sum of rise T_{rise} and fall time T_{fall} of the signal. T_{rise} only depends on the PMT construction parameters while the T_{fall} depends on the signal amplitude V_{max} and the time constant $\tau_{fall}=C_{PMT}R$ of discharge of the PMT capacitance C_{PMT} on the output resistor R.





Using the capacitance discharge law $Q=Q_0e^{-t/\tau fall}$

$T_{fall} \sim V_{max}/Thr \sim Q_0/Q(ToT) \sim K_1e^{ToT/\tau fall}+K_2$

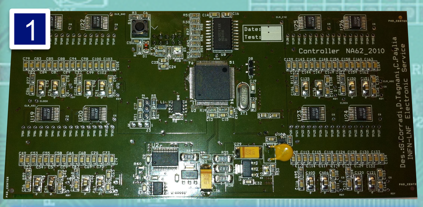
The actual relation Q(ToT) can be obtained using a fit to the distribution of Q vs ToT. This relation is in principle the same for all the LAV PMT's

The sensitivity of the method is reduced at high charge due to the exponential dependence of Q from ToT.

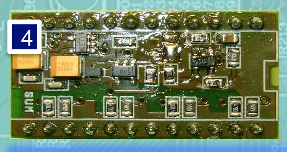
Charge reconstruction in NA62 LAV

- ☑ Study the ToT vs Charge using a QDC and TDC
  - Only during calibration and not during experiment
- ☑ Fit the function Q(ToT) (i.d. polinomial function)
- ☑ Measure the time using a TDC only (during data taking)
- ☑ Use the Q(ToT) function to get the charge directly in digital readout board FPGA

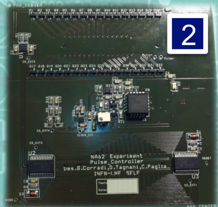
FEE board



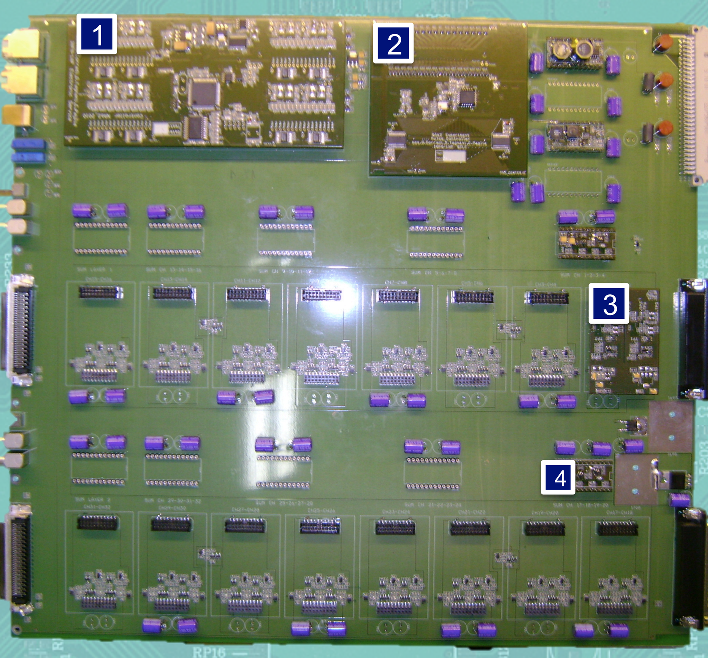
1 Board controller
Communicate using CANOpen
Allows to setting and reading:
Thresholds (set/read)
Power connection (read)

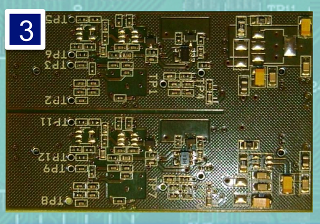


4 Sum mezzanine card
Sum 4 analog ch
Sum 16 analog ch (sum of sum)
Connected to a 50Ω lemo out



2 Test pulse controller
Can set for each channel:
Pulse height (set/read)
Pulse width (set/read)
Pulse rate (set/read)





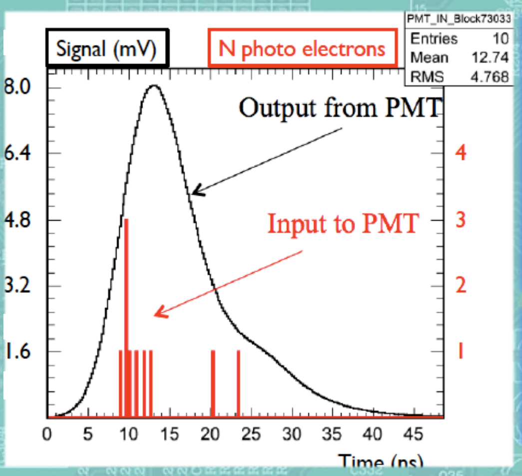
3 ToT mezzanine card
2ch and 2 thr per board
Include the circuits for
Clamp
Amplifier
Comparator & LVDS driver

Inputs	Type	Outputs	Type
Power connection	VME J1	64 LVDS output	2xSCSI2
32 analog signals	2xDB37	8 analog sums of 4 ch	8xLEMO-00
		2 analog sum of 16 ch	2xLEMO-00
1 CAN OPEN	RJ11	1 CAN open	RJ11

9U Boards components	# of pieces
±6 V voltage regulator	4
Time over threshold Mezzanine (2ch)	16
Sum of 4 mezzanines (8 sum 4 + 2 sum 16)	10
Board controller	1
Test signal generator	1

Simulation

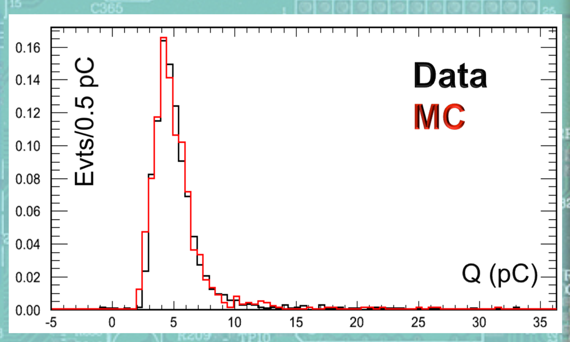
Digitization simulation



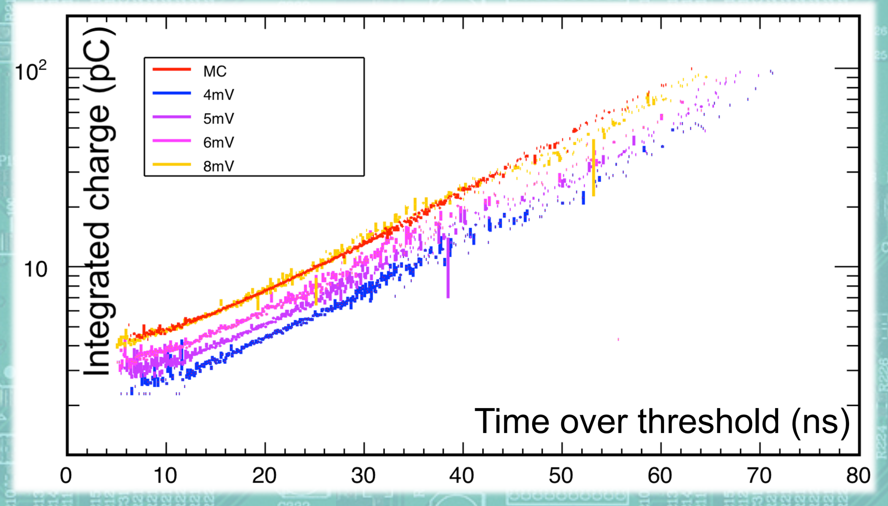
PMT simulation correctly treats:
- Path fluctuations for optical photons
- PMT Photocathode QE(λ)
- Dynode by dynode gain fluctuations

Front end electronic simulation includes
- Cable length simulation
- Threshold simulation
- Hysteresis simulation

INPUT to simulation from GEANT4
Number of photons in each event
Arrival time of each photon
Photon wavelength



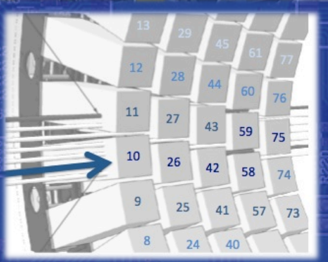
Digitization simulation OUTPUT
1) Photomultiplier analog signal
   - Reproduce amplitude and shape
2) Photomultiplier total charge
   - Reproduce the MIP total charge and fluctuations
3) Montecarlo Q vs ToT curve
   - Reproduce the MIP Q vs ToT measured
   - Comparison with different thr data set obtained during test beam shows good agreement with nominal thr value only



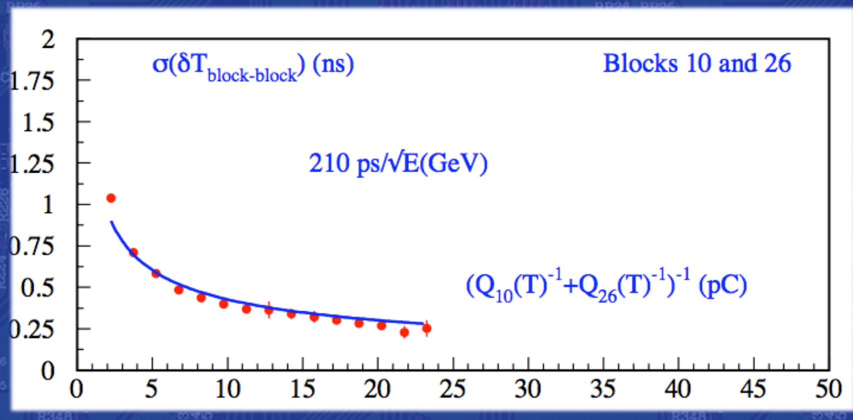
Performance

Test beam setup of the ANTI-A2 @ CERN T9 beam

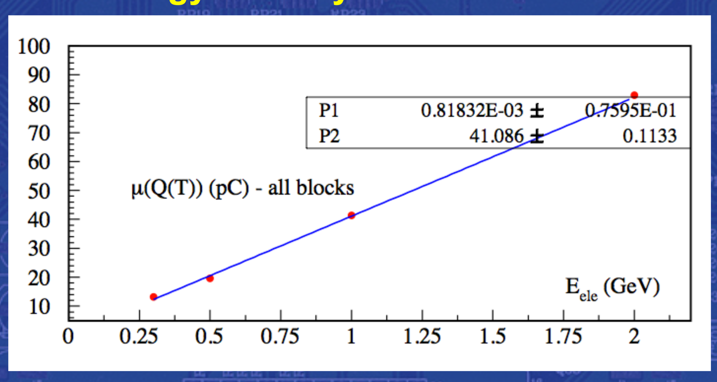
Test beam T9 9/2010
- ☑ Mixed hadron beam e μ π up to 7 GeV
- ☑ Trigger by scintillators on beam line
- ☑ Cherenkov based beam PID (tag e⁻)
- ☑ 6 prototypes VME 6U board tested (96 ch)
- ☑ Read out with commercial QDC and TDC
- ☑ First tests of TELL1 and TDC only readout



Time resolution



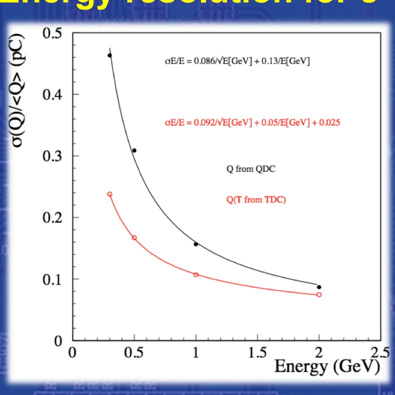
Energy linearity for e⁻



Energy and time resolution are dominated by detector performance:

Energy resolution dominated by shower containment
Time resolution dominated by spread on time of arrivals of photons to the photocathode

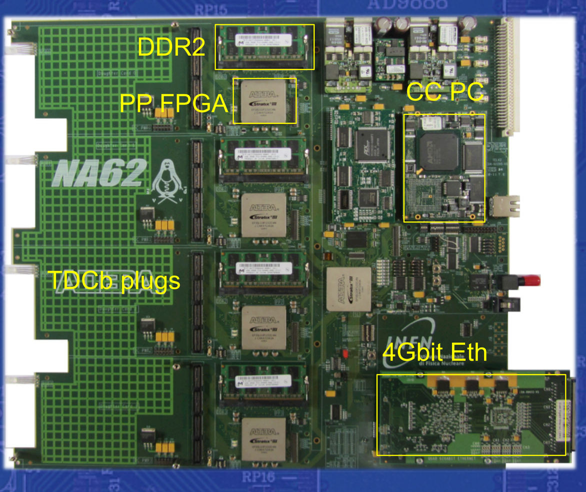
Energy resolution for e⁻

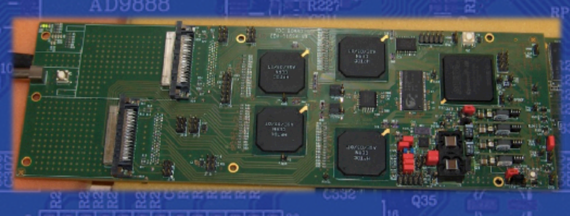


TDC & Tel62

TEL62 readout board

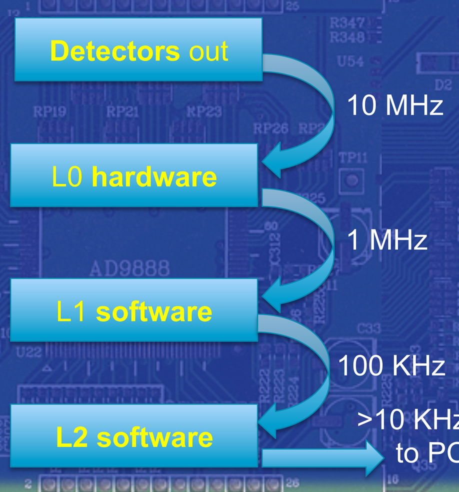
- ☑ Common digital readout board TEL62 (based on LHCb TELL1)
- ☑ 4 slots for custom mezzanine boards
- ☑ 1 FPGA/slot with 2Gbyte DDR2 memory
- ☑ Up to 516 TDC channels per board (in 4 TDCb mezzanine)
- ☑ 4x1Gbit eth connection to the readout PCs
- ☑ On-board credit card PC for remote programming and control
- ☑ TTCex clock reciever





TDC mezzanine board

- ☑ Based on CERN HPTDC chip
- ☑ Up to 128 channels per mezzanine board
- ☑ LSB down to 100ps and leading and trailing measurement
- ☑ Nominal TDC time resolution < 50 ps
- ☑ On board trigger matching mode available



LAV in NA62 Trigger

- ☑ Used to reject the $\pi^+\pi^0$ events with photons at large angle
- ☑ Flag photons into LAV and keep random veto (<1%)
- ☑ Level-0 implemented in TEL62 hardware FPGA
  - e.g. CHOD,RICH, Muon veto, LKr veto, LAV A12 veto
- ☑ Level-1, γ veto using the full LAV detector 12 stations
  - Software implemented
- ☑ Level-2, implemented in software
  - LAV not used anymore

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