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Conceptual Design of 3D Integrated Pixel Sensors for the Innermost Layer of the ILC Vertex Detector

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The paper presents a design of CMOS Pixel Sensor (CPS) using the vertical integration technology (3DIT), expected to alleviate the most essential limitations of 2D-CPS. Our objective is to develop an intelligent architecture in order to meet the requirements of the innermost layer of the International Linear Collider (ILC) vertex detector, which are particularly demanding in spatial resolution and associated readout speed. The sensor, with a pixel pitch of 23 μm, will be composed of 3-tiers Integrated Circuits (IC) with different functionalities: detection with in pixel analogue processing, pixel-level 3-bit Analogue to Digital Conversion (ADC) and fast parallelism sparse readout.

Summary 500 words

The innermost layer of the ILC vertex detectors requires pixel sensors with a high spatial resolution (< 3 μm) associated with a very demanding readout speed (~< 10 μs). Although 2D CMOS Pixel Sensors (2D-CPS) with column-level ADCs can realize such a good spatial resolution, they still have inherent limitations that make it difficult to achieve simultaneously short frame readout times. The 2D-CPS operates in a "rolling shutter" mode, where the amplified pixel signals are routed row by row to the periphery of the pixel matrix for a sparse readout. The global row-wise sequential processing of the pixel matrix becomes a bottleneck when trying to reduce the readout speed. Using 3DIT, two or more pixellised chips can be vertically interconnected. Therefore the amount of processing per pixel can be increased. This approach does not only improve material budget by eliminating the insensitive periphery of a coarse 2D-sensor, it also allows to meet the requirement of high readout speed by replacing the global row-wise sequential processing used in 2D-CPS with a parallelised readout architecture. The parallelism consists in splitting the pixel array into several sub-matrices, each operated independently in "rolling shutter" mode. The time to read all the rows in every sub-matrix is then reduced. Moreover, each pixel integrates a 3-bit ADC to guarantee the required spatial resolution. This efficient use of the parallelism can also reduce global power consumption for a large-scale array.
In this paper, we propose a 3D-CPS device which will be composed of three tiers: In the bottom tier, the pixel contains a sensing diode and an in-pixel amplifier associated with a correlated double sampling (CDS) processing. In the intermediate tier, it is composed of a 3-bit single-slope pixel-level ADC. Digital outputs of each ADC connect vertically to the top tier, which performs a sparsified data readout. All of these pixel functions are integrated in a pitch of 23 μm. In order to demonstrate the advantages of such an intelligent architecture of 3D-CPS, a standard 2D prototyping chip was submitted to verify its basic functionality as the first step. In order to improve the spatial resolution, the Least Significant Bit (LSB) of the pixel-level ADC should be at approximately the same level as the voltage resulting from the noise of pixel sensors. A circuit containing the pixel-level ADCs and the pixel-level sparse readout has been submitted. These two blocks have been tested and evaluated separately. The measurement results show that the proposed pixel-level ADC fulfils the requirement in terms of noise, dynamic range, nonlinearity and power consumption. A faithful functionality of the pixel-level sparse readout has also been verified experimentally. The flexibility and adaptability of the approach followed make it very simple for realizing real 3D-CPS devices in near future.

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