News on the 130 nm technology support

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130 nm technology

- Foundry services & Technology technical support provided by CERN.

CMOS 8RF-DM

Low cost technology for ***Analog & RF*** *designs*

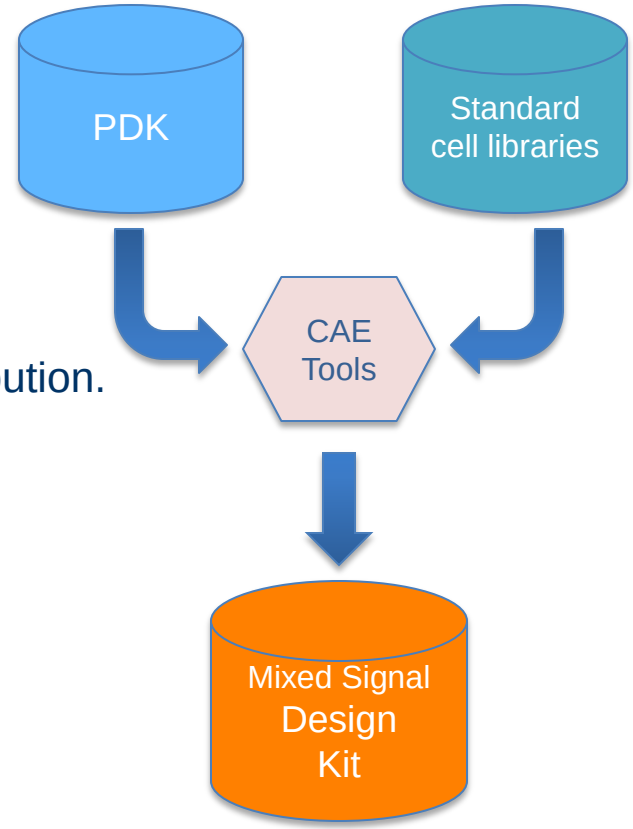
CMOS 8RF-LM

Low cost technology for ***Large Digital*** *designs*

- Mainstream technology is CMOS8RF-DM
  - Full support: CERN compiled Mixed-Signal design kit
- Secondary stream is CMOS8RF-LM
  - Full support for in-house on-going projects: CERN compiled Mixed-Signal design kit
  - not recommended for new designs

CMOS8RF Mixed Signal design kit

- Mixed Signal Kit V1.8
  - Based on foundry PDK V1.8.0.1
  - Released middle this year - 11/6/2011
  - Foundry Standard cell and IO pad libraries
  - Versions of CAE Tools
    - Compatible with the *"Europractice" 2011* distribution.
    - Open Access database.
  - Bug fixes and Important updates.
    - *Original IBM PDK 1.7.0.x had several tools compatibility problems*
  - Support for LINUX Platform
    - Qualified on RHEL4 & RHEL5

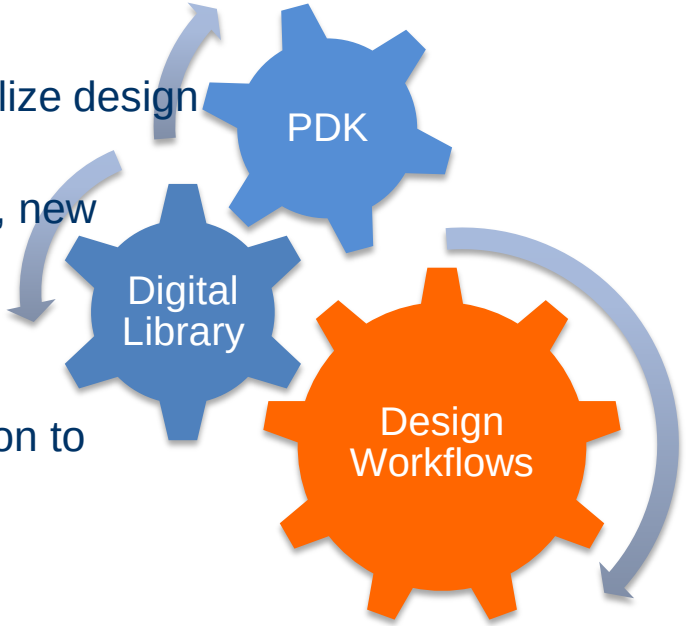


- **New patch release based on IBM PDK 1.8.0.4 to be available soon**

- Two design kits available:
  - CMOS8RF-DM (3-2-3 BEOL)
  - CMOS8RF-LM (6-2 BEOL)

CMOS8RF Mixed Signal - remarks

- Rules
  - Keep given major release as long as possible, to stabilize design process of many project teams
  - However, if new original PDK contains critical updates, new Mixed Signal PDK major release is inevitable



- Certification process
  - Depending on changes in original new PDK adaptation to Mixed Signal PDK
    - Is done in-house *(some time is needed)*
    - Development work subcontracted to Cadence, VCAD design services *(more time needed! Ex. 2 months)*
    - Close collaboration of CERN - VCAD – IBM

- Original IBM PDK patches are always available on our web-site immediately after release
  - It is strongly recommended to not apply these to Mixed Signal PDK – wait for patch release from CERN

Design Kit Distribution

No change in rules

- The Mixed Signal Design kit is available to collaborating institutes.
  - Distributed to 28 Institutes and Universities
  - No access fees required.
  - Pay-per-use scheme.
    - A 7% fee is applied on the fabrication cost (prototyping, production).
    - This fee covers part of the design kit maintenance costs.

- For New Users
  - To acquire the CMOS8RF Mixed Signal Design Kit
  - Contact Wojciech.Bialas@cern.ch
    or Kostas.Kloukinas@cern.ch
  - Establish a CDA with foundry (if not already in place).
  - Granted access to the CERN ASIC support web site.

CMOS8RF digital libraries

- Currently Available
  - Regular-Vt core cells
  - Short-IO Inline, wirebond, Pads

- Future Plans – *driven by user demand*
  - Regular-Vt core cells at lower supply voltages (1.0 V, 0.8 V)
  - High-Vt core cells, for low power designs.
  - “Compact layout” core cells.
  - Rad-Tolerant cells: ex. DICE

- Work items
  - Layout design
  - Library characterization
  - Design kit integration
  - Digital back-end flow adaptation

THANK YOU