A Low-Power Wave Union TDC Implemented in FPGA

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A low-power time-to-digital convertor (TDC) for an application inside vacuum has been implemented based on the Wave Union TDC scheme in a low-cost field-programmable gate array (FPGA) device. Bench top tests have shown that a time measurement resolution better than 30 ps (standard deviation of time differences between two channels) is achieved. Special firmware design practices are taken to reduce power consumption. The measurement indicates that with 32 channels fitting in the FPGA device, the power consumption on the FPGA core voltage is approximately 9.3 mW/channel and the total power consumption including both core and I/O banks is less than 27 mW/channel.

Summary 500 words

The mu2e experiment in Fermilab requires operating a large channel-count straw tube chamber system inside vacuum demanding low-power consumption on all stages of readout electronics including the TDC device. The time difference of signals detected at both ends of a straw tube is measured to a precision better than 35 ps so that the charged particle hit location along the tube length can be determined. This required time resolution is much finer than that of typical straw tube TDC in which 1-2 ns is sufficient.

The Wave Union TDC is a scheme developed in our previous work to improve resolution of TDC implemented in FPGA beyond its cell delay. Multiple 0-1 and 1-0 transitions are generated in the delay chain in the Wave Union TDC and registered for encoding, which effectively provides multiple measurements with one set of delay chain and register array structure and thus improves time measurement resolution. (Regular TDC's make one measurement with a single 0-1 transition.) Intrinsically, the Wave Union TDC is a low-resource and low-power consumption scheme since less logic elements are used comparing to typical TDC schemes in order to achieve a finer resolution.

In addition, special digital design practices are taken to properly interface fast clock (250 MHz) and slow clock (62.5 MHz) domains so that in each channel, the fast clock is confined in the register array used to capture wave union transitions in the delay line while most encoding and data handling blocks are put in slow clock domain. Taking advantage that the required minimum double hits separation is relatively large, encoders and other common functional blocks are shared among multiple channels to further reduce logic element usage and power consumption.

A low-power edition of the Wave Union TDC has been developed in an Altera Cyclone III FPGA device (EP3C25F324C6, $73.90 as of Apr. 2011) and tested in a Cyclone III FPGA evaluation board. Even under conditions of using switching power supplies provided on the evaluation board and having single ended signal connections between the FPGA and other devices, a time measurement resolution of 30 ps (defined as standard deviation of time differences between two channels with constant relative delay) is achieved.

To evaluate power consumption, 32 TDC channels are fit into the FPGA, which take 56% of logic elements in the device and currents in power nets for both FPGA core and I/O bank are measured. In normal operating condition, the current in the 1.2V net supplying the FPGA core is 0.23 to 0.25 A that yields 276 to 300 mW for 32 channels and 8.6 to 9.3 mW/channel. The 2.5V I/O bank power supply draws 0.17 to 0.22 A that consumes 425 to 550 mW for entire chip. Therefore in this test the total power consumption is 22 to 27 mW/channel, including both FPGA core and I/O banks. It can be seen that the core power consumption has already been reduced significantly lower than the one in I/O bank with 2.5V I/O standards (LVDS, 2.5V etc.). Further reduction of total power can be anticipated when I/O standards at lower voltage are utilized.

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