

DAQ systems for 10^8 channels detectors: design and system level simulations

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Calorimeters for a future International Linear Collider developed within the CALICE collaboration will feature about 10^8 channels. A scalable control and data acquisition system was developed. It is based on GigaEthernet and a specific serial link packing slow control, fast control and read out data. Most of the hardware and firmware components are shared among the various detectors. The first prototype will be presented. Its extrapolation for a 10^8 channels detector requires stringent optimization studies about architecture and structural parameters. A first approach about specific tools for system level simulation based on SystemC and TLM technologies and their coupling to physics simulation and analysis environment will be presented.

Summary 500 words

The CALICE collaboration proposes various kinds of calorimeters to be candidates for a detector for a future International Linear Collider. Those calorimeters provide tracking capabilities thanks to granularities which can exceed the LHC standards by three orders of magnitude. Thus for the CALICE silicon-tungsten electromagnetic calorimeter, 10 000 channels are expected in only one cubic decimeter.

For such a density of channels, the power consumption (power pulsing technique), the integration and the huge dataflow require specific control and data acquisition electronics. The system is being developed and is at its first prototyping stage. The very first test beam with a 80 000 channel hadronic calorimeter are foreseen for June'11.

For the prototyping, the various elements are based on programmable technologies while the detectors are equipped with ASICs (LAL/OMEGA) sharing the same digital control interface. The concept of a scalable, flexible, and compact architecture was developed by Manchester University, UCL and Cambridge University and LLR. The system architecture is similar to a computing network with 3 levels of switches. It relies on standard GbEthernet technologies at upper level and proprietary serial link close to the detector. The proprietary serial link derives from FastEthernet and provides 16b/20b encoded data packing together slow control, fast control and data acquisition in the same protocol and medium.

Starting from the detector, the first layer is the detector interface (DIF) connected to a second layer for data concentration (DCC, similar to a hub function) which communicates with a Local Data Aggregator (LDA, similar to an Ethernet switch).

The DIF is a very local node which can manage about 10^4 channels. It interconnects several chains of front-end ASICs to the proprietary serial link and USB for debugging. The various protocols are translated and data packets are managed thanks to two levels of buffering and the appropriate logic. DIF provides an access to user data storage functions (registers, ram, external flash). HDL code is shared among detectors.

At a detector module level, the DCC will fan-out and aggregate packets handling up to 9 DIFs (10^5 channels). Packets are queued, multiplexed and buffered. Finally the LDA will serve up to 10 DCC providing Giga-Ethernet connectivity to the PC farm.

The proprietary serial link (3 differential pairs) is fully bidirectional for slow control and read-out. Fast control is provided using specific control characters multiplexed in the data flow itself. For specific test modes, 2 pairs are added for an external trigger and a busy signal from the detector.

Extrapolating this first prototype system to an optimized system for a 10^8 channel detector is not straightforward. Specific tools for system level simulation based on SystemC and TLM technologies have been setup in order to study architectural options (number and size of data queues and buffers, overall architecture). They can be coupled to physics simulation (GEANT4) and ROOT analysis environment in order to provide reliable results. A first approach and preliminary results will be presented.

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