

# Wideband (500 MHz) 16 bit Dynamic Range Current Mode Preamplicifier for the CTA cameras

*Tuesday, 27 September 2011 15:40 (25 minutes)*

A wideband current mode preamplifier with 16 bits dynamic range (DR) is presented. It has been designed for the cameras of the Cherenkov Telescope Array (CTA). A novel current division scheme at the very front end part of circuit splits the input current in to two scaled currents which are connected to independent current mirrors. The mirror of the high gain path comprises a saturation control circuit for accurate current division. Measurement results of an ASIC (Austriamicrosystems 0.35  $\mu\text{m}$  SiGe technology) are presented: 500 MHz BW, 16 bits DR, 10 pA/sqrt(Hz) input referred noise and relative linearity error below 3%.

## Summary 500 words

The fast readout option (1 to 2 GS/s) of the Cherenkov Telescope Array (CTA) project needs a wideband, high dynamic range and low noise preamplifier, in order to readout a PMT which operates at low gain (40 K) to avoid ageing problems. A 16 bit dynamic range (DR) is required on the one hand by the measurement of the single photo-electron signal (SPE) for calibration purposes, and on the other hand by the highest light pulse (5000 PE). Good SPE resolution at this gain imposes low noise requirements as well: 10 pA/sqrt(HZ) for a current mode readout. Low input impedance and low voltage operation are required.

Current mode circuits, based on super common base or regulated cascode stages are well suited to fulfill most of previous requirements. Current mode circuits usually create multiple gain paths using a current mirror to replicate the input current with different scaling factors. However, large currents saturate the input branch of the mirror and DR is in practice limited to 14 bits or less.

We propose a novel current mode circuit to overcome the maximum signal limitation by creating multiple gain paths at the very front end of the input stage. The input current is split in the common base input stage in two (or more) output scaled currents. Cascode techniques are used to improve the accuracy of the current division by increasing the output impedance of this stage. Voltage feedback (A) is used to decrease the input impedance.

The outputs of this stage are connected to independent current mirrors. These are low voltage cascode current mirrors with a common base transistor for local feedback to minimize input impedance and so the voltage variation the input nodes (output nodes of the current division common base stage). In addition, the high gain (HG) current mirror comprises a saturation control circuit.

Large input currents could provoke large variations in the voltage at the input node of the high gain (HG) current mirror. To avoid this, the HG comprises a fast saturation control circuit which quenches the excess current in case of large currents.

A first prototype (called PACTA) of the CTA preamplifier including the inventions described above (patent application ES 201130565) has been designed in Austriamicrosystems 0.35  $\mu\text{m}$  SiGe BiCMOS technology. A pseudo-differential input stage is used to minimize the effect of common noise. A fully differential transimpedance amplifier is connected to each HG and LG mirrors.

Measurements results are:

Input Referred Noise: 300 nA rms.

SNR for SPE spectra: 8, at the nominal PM gain (40K).

Input range: > 20 mA peak.

Dynamic range: 15.9 bits.

High Gain: 900 Ohm. Saturation at 1 to 1.5 mA peak.

Low Gain: 45 Ohm. Full DR.

Relative linearity error for charge measurements: < 2 %. Integral of the pulse.

BW: 500 MHz. Both for HG and LG.

Input impedance: 10 to 15  $\Omega$ . For full BW.

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**Session Classification:** A2 - ASICs

**Track Classification:** ASICs